1. (25%) Please **mark** 1A(a), 1A(b), ..., 1A(e), 1B(a), and 1B(b), respectively, in top of your answers.

(1A) In a typical driver circuit as shown in Fig. 1, the zener diodes D_z are ideal with zener voltage V_z = 5.3 V and forward cut-in voltage V_γ = 0.7 V. The operational amplifier is ideal too. The BJTs, Q_N and Q_P, can be modeled by $|V_{BE(on)}|$ = 0.7 V. The power supply is V_{CC} = 15 V. The resistors are R = 1 kΩ and R_L = 10 Ω. The switch SW can be selected either in position 1 or position 2. A current signal I_i with average I_{av} and peak-to-peak I_{pp} is applied to the input.

(a) When SW is at position 2, **find** the small signal gain V_L/I_i. **(3%)**

(Case 1) When I_i is a saw-tooth waveform with I_{av} = 0 and I_{pp} = 10 mA,

(b) plot the waveform of V_L for SW being at position 1. **(3%)**

(c) plot the waveform of V_L for SW being at position 2. **(3%)**

(Case 2) When I_i is a saw-tooth waveform with I_{av} = 0 and I_{pp} = 20 mA,

(d) plot the waveform of V_L for SW being at position 1. **(3%)**

(e) plot the waveform of V_L for SW being at position 2. **(3%)**

Note: Be sure to properly indicate the voltage values in your plots.

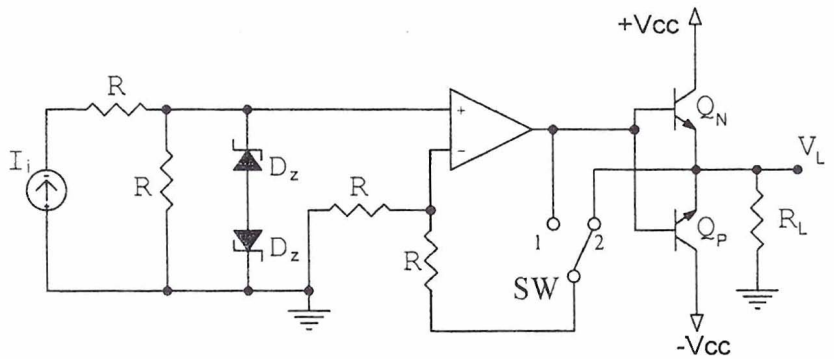


Fig. 1

(1B) A Si-BJT with β = 100 and r_o = ∞ is used to make a common emitter amplifier biased by a constant current source as shown in Fig. 2. The capacitance C is very large.

(a) Sketch the small signal equivalent circuit for this amplifier using hybrid-π-model. **(4%)**

(b) If a voltage gain of V_o/V_i = –200 is desired, **find** the value of I_Q and the input resistance R_{in}. **(6%)**

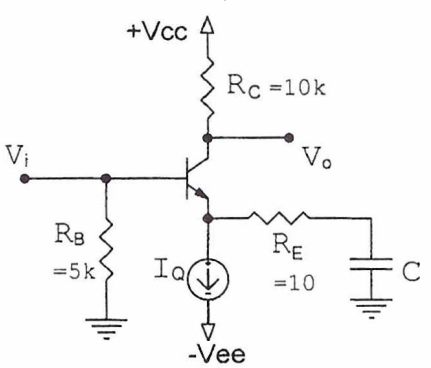


Fig. 2

2. (25%) A 2-stage amplifier with an equivalent circuit is shown in Fig. 3. Let A_{v1}=100, A_{v2}=100, C_1=C_2=0.1pF and the resistance at node X, Y are R_X=R_Y=1MΩ.

(a) If C_M=*0*, **write** down the transfer function of the overall gain, $A_v(\omega)$. **(5%)**

(b) Sketch both the gain and phase Bode plots of this amplifier. **(5%)**

(c) With Miller compensation, C_M=*10pF*, **find** the new dominant pole, ω_{pD}. **(5%)**

(d) Sketch the Bode plots (gain and phase) of the amplifier with C_M=*10pF*. **Estimate** the unity gain bandwidth and the phase margin, ϕ_M and label them in your plots. **(10%)**

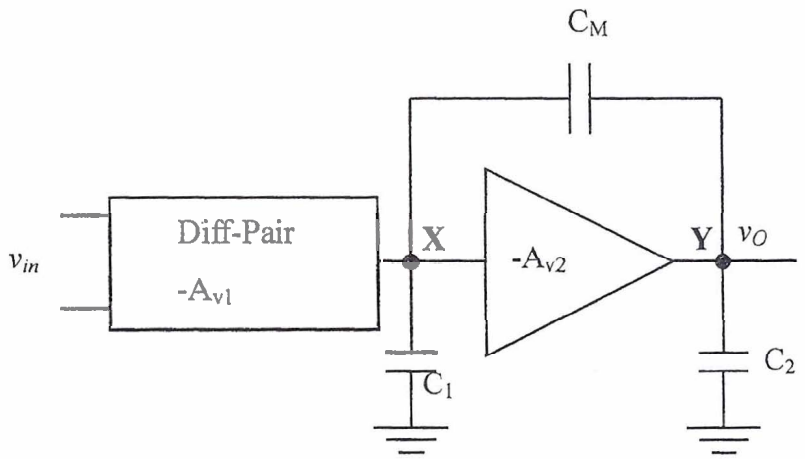
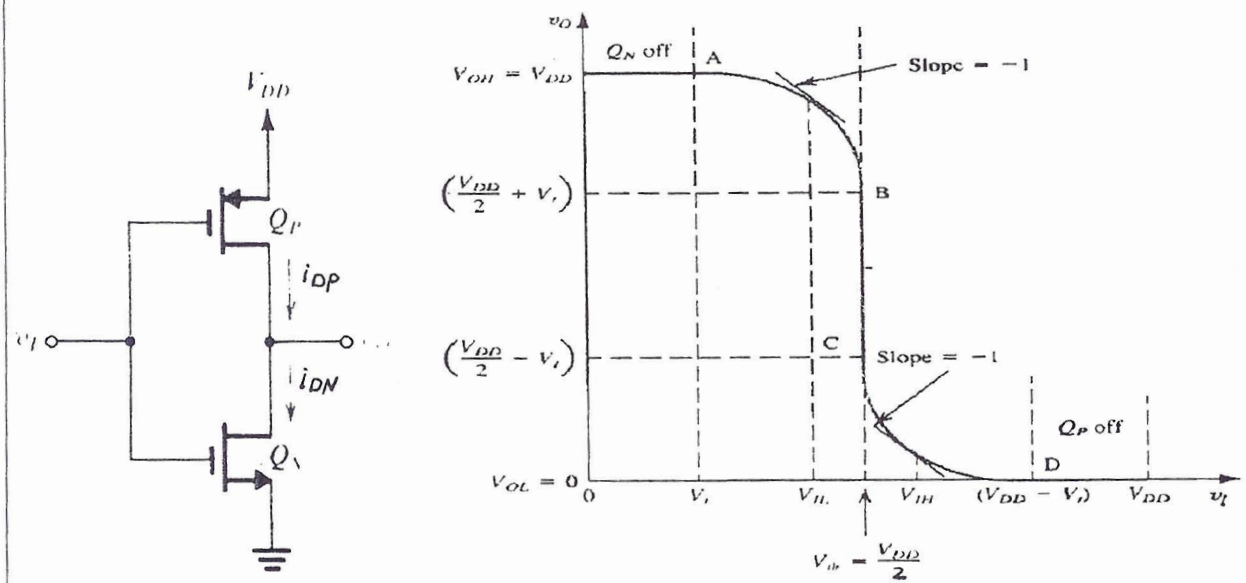


Fig. 3

3. (25%)

(a) For a CMOS linear amplifier as shown below, what **are** the operation modes of Q_N and Q_P in BC and CD regions, respectively? (Ans: off or triode or saturation)? **(8%)**



(b) As shown above with v_I=0 V, please **sketch** the i_{DN} and i_{DP} vs v_O curves. Please **indicate** the operation point and V_{OH}. **(9%)**

(c) In memory circuit, **should** the Word and Bit lines be connected to source/drain, gate, or substrate of MOSFET, respectively? **(4%)**

(d) What **are** the approximate dimensions (in cm) of channel length and gate oxide thickness of MOSFET in current VLSI, respectively? **(4%)**

4. (25%) Consisted of a Schottky diode, two resistors, and three BJTs, a modified ECL with three inputs *A*, *B*, V_R and an output *C* is described as follows. Two primary inputs *A*, *B* and a reference voltage V_R are connected to the bases of BJT Q2, Q1, and Q3, respectively; All the emitters of BJT Q1, Q2, and Q3 are connected to node *E*, and the first resistor R_E are wired between node E and ground; Both the collectors of BJT Q1 and Q2 are wired to power supply *Vcc*, while the collector of BJT Q3 is the output *C*. The Schottky diode and the second resistor R_C are wired in parallel between power supply *Vcc* and output *C*.

(a) Please **draw** this modified ECL circuit. **(10%)**

(b) **Write** the output function *C* in terms of inputs *A* and *B* with brief explanation. **(6%)**

(c) **Find** voltages of V_R, logic-0 and logic-1 in terms of *Vcc* and $V\gamma$, where $V\gamma$ is the turn-on voltage of the Schottky diode. **(9%)**