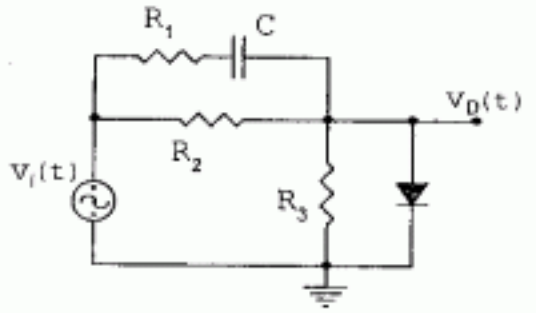
國　立　清　華　大　學　命　題　紙

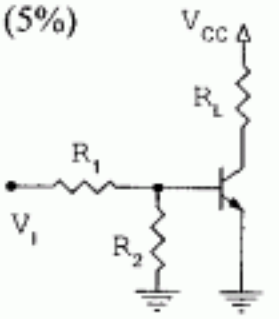
九十三學年度 電機工程學系甲、乙組 暨 光電工程研究所 碩士班入學考試

科目 電子學 科號 2603、2702、2803 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

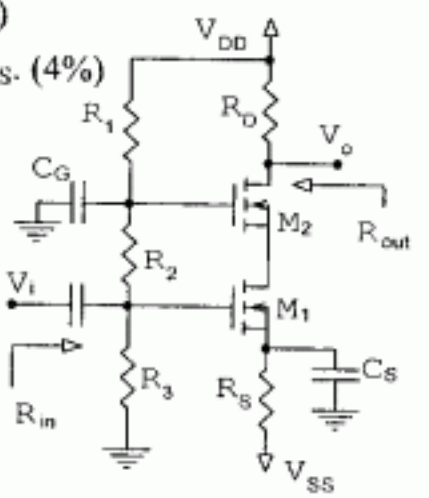
1. The p-n junction diode in the circuit can be modeled by a constant voltage drop of $V_\gamma = 0.7$ V when it is forward biased. The input voltage is $v_i(t) = V_{i,dc} + V_{i,ac}\cos(\omega t)$ with $V_{i,ac} = 20$ mV. The capacitor is $C = \infty$. The resistors are $R_1 = R_2 = 10$ kΩ, $R_3 = 5$ kΩ. The diode voltage is $v_D(t) = V_{D,dc} + V_{D,ac}\cos(\omega t)$.
   (1) Find the values of $V_{D,dc}$ and $V_{D,ac}$ when $V_{i,dc} = 20$ V. (5%)
   (2) Find the values of $V_{D,dc}$ and $V_{D,ac}$ when $V_{i,dc} = -20$ V. (5%)



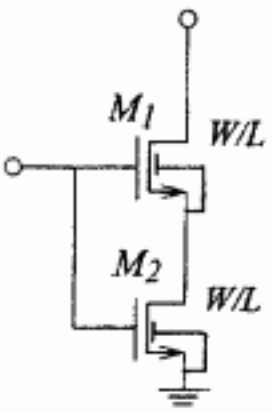
2. A power BJT with current gain β=50, base-emitter turn-on voltage $V_{BE(on)}$=1 V, collector-emitter saturation voltage $V_{CE,sat}$=0.5 V is used in the switching circuit as shown. The component parameters are $R_1 = R_2 = 10$ kΩ, $R_L = 200$ Ω and $V_{cc} = 12$ V.
   (1) Find the minimum value of V_I that the BJT is saturated. (5%)
   (2) Find the maximum value of V_I that the BJT is cutoff. (5%)
   (3) Determine I_C and V_{CE} for $V_I = 12$ V. (5%)



3. In the amplifier circuit as shown, the MOSFET M_1 and M_2 are biased properly and having a given transconductance g_m.
   (1) Sketch the small signal equivalent circuit using low frequency π model of MOSFET. (3%)
   (2) Find the expressions for V_o/V_i, R_{in} and R_{out}. (3%)
   (3) Explain the functions of the capacitors C_G and C_S. (4%)

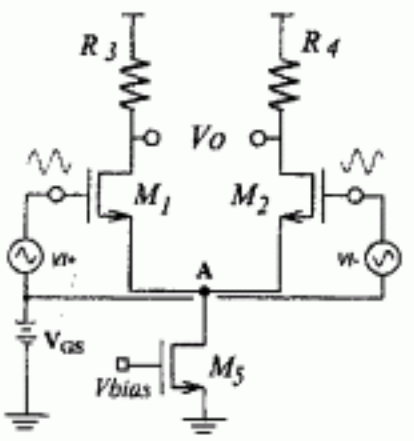


4. This is a cascode configuration, also named as Sooch' cascode.



In this configuration two identical devices are cascoded with their gate connected together. If you can neglect the body effect, please prove the circuit is equivalent to the single device with the same width (W) and double length (2L). (15%)
(hint: you firstly have to identify the operation of each transistor)

5. This is a differential amplifier. Two differential paths can be treated as perfect match, that is, R3=R4, M1=M2.



(a) Please draw the differential and common mode small signal model, and calculate the voltage gain in each case. (12%) (hint: you have to derive the small signal parameters before gain calculation)

(b) If input is differential sinusoid, please draw the node A waveform under two cases. One is output signal not being saturated. The other is output signal has been saturated. Explain your reason. (8%)

6. (15%) Without any input, a circuit with one capacitor, one Op Amp, and three resistors is described as follows. A capacitor with value C_1 connects to ground and the negative-input of the Op Amp. The first resistor with value R_1 connects to the negative-input and the output of the same Op Amp mentioned before. The second resistor with value R connects to the positive-input and output of the same Op Amp mentioned before. The third resistor also with value R connects to the positive-input of the same Op Amp mentioned before and the ground. The Op Amp mentioned before has maximum saturation output voltage Vp and minimum saturation output voltage –Vp. Given the general equation for the voltage across a capacitor in an RC network below, and answer the following questions

$$V(t)= V_{final} + (V_{initial} - V_{final})\exp(-t/(RC))$$

(a) Draw the diagram of this circuit. 5%

(b) Find the waveform and its period in the output of the Op Amp. 10%

7. (15%) A conventional CMOS logic gate with NMOS connections described as follows. The first NMOS transistor named N1 connects to ground with source end, to primary input A with gate end, and to the source end of another NMOS transistor named N2 with drain end; The second NMOS transistor named N2 connects to primary input B with gate end, to the drain end of another NMOS transistor named N1 with source end, and to the primary output F with drain end; The third NMOS transistor named N3 connects to ground with source end, to primary input C with gate end, and to the primary output F with drain end. The power supply, inputs' frequency, output's frequency, and output capacitance are VDD, f_i, f_o, and C, respectively. If NMOS conduction parameter Kn, PMOS conduction parameter Kp, the NMOS threshold voltage Vtn, and the PMOS threshold voltage Vtp are all given, please answer the following questions.
   (a) Draw the diagram of the PMOS connections. (5%)
   (b) Find the logic function F=? (5%)
   (c) Find the dynamic power dissipation of this logic gate. (5%)