1. Short questions:

(a) For high quality Si layer with low doping at room temperature, writer down the following physical quantities: (1) energy bandgap, (2) electron mobility and hole mobility, (3) intrinsic carrier concentration, (4) relative permittivity. (10%)

(b) Write down the formula for resistivity. Estimate the resistivity of n type polysilicon doped to $10^{20}cm^{-3}$, assuming an electron mobility of 100 $cm^2V^{-1}S^{-1}$. (3%, 2%)

(c) Estimate the dielectric relation time of an n type silicon sample doped to $10^{16}cm^{-3}$. Only an ordre-of-magnitude estimate is required. (5%)

(d) For a trap-free semiconductor, write down the five Shockley semiconductor equations. You need to describe the symbols that are used in your equations. (10%)

2. For an npn bipolar junction transistor the emitter doping concentration is $N_{dE}$, the base doping concentration is $N_{aB}$, and the collector doping concentration is $N_{dC}$.

(a) Fill the proper symbol (<<, <, =, >, >>) into the following parentheses (5%)
$N_{dE}$ ( ) $N_{aB}$ ( ) $N_{dC}$.

(b) Explain the reason for making the choice in part (a). (10%)

(c) If the base is non-uniformly doped there is a doping gradient in the base, which direction do you prefer? Collect-side concentration higher than the emitter -side concentration or vice versa? Why? (5%)

3. Plot the cross section of a real n-channel J-FET with $p^+$-substrate and n-epi layer. (5%) Draw the low-frequency small-signal equivalent circuit of this J-FET, take the source and drain terminal resistance into consideration. (5%) Draw the high-frequency small-signal equivalent circuit of this J-FET. (5%)

4 . For a p-channel MOSFET, with p+ poly-silicon gate,

(a) If the source, drain and substrate are all connected to ground and gate is connected a ramp voltage source, plot qualitatively the typical low-frequency C-V curve in reference to zero gate bias. (5%)

(b) For three transistors with identical layout geometric and fabrication process except for different channel doping levels, $N_{d1}$, $N_{d2}$, $N_{d3}$ with $N_{d1}=10N_{d2}=100N_{d3}$, for device A, B, C respectively, plot qualitatively three corresponding high-frequency C-V curves of the three device on the same plot, please label them properly. (5%)

(c) On the same plot, compare the C-V curves of transistors with and without poly-depletion effect? Will this effect be more or less significant with device scaling? Why? (5%)

(d) Proposed a method to measure the overlap capacitance between source/drain and gate of this device. (5%)

5.

(a) For a MOS-C with with n+ poly-Si gate plus p-type substrate, plot the energy band diagram when the gate-to-substrate voltage equals the threshold voltage. Write down the threshold voltage equation and label each term you used in the plot. (10%)

(b) Explain why the drain current saturates after channel pinch-off in a MOS transistor. (5%)