1. (10%) Consider the representations of the floating-point numbers.
   A number is often denoted as $(-1)^S \times F \times 2^E$. What are the English names and meanings of F, and E, respectively? (5%)
   In the IEEE 754 standard format, a number is denoted as $(-1)^S \times (1+F) \times 2^{(E-Bias)}$. For single and double precision numbers, what are the values of *Bias*, respectively? (5%)

2. (15%) Explain the meaning of each of the following MIPS instructions using an *if-statement*. Denote the program counter as *PC* when needed. Note that an instruction has four bytes.
   slt $s1, $s2, $s3 (5%)
   slti $s1, $s2, 100 (5%)
   bne $s1, $s2, 25 (5%)

3. (10%) In a 5-staged pipelined computer, 20% of the instructions are assumed to be branch instructions that could cause one-cycle pipeline stalls, if not properly handled.
   (a) Ignoring all other hazards, what is the CPI of this computer by taking into account this branch-related control hazard? (5%)
   (b) If the probability of a branch instruction being taken is 30% on the average, then what is the average CPI under the "*predict-not-taken*" branch prediction scheme? (5%)

4. (20%) Consider a computer system with a cache of 4K blocks, a four-word block size, a 4-byte word size, and a 32-bit address.
(a)What are the total number of sets and the total number of tag bits for caches that are (i) direct-mapped, (ii) two-way set associative, (iii) four-way set associative, and (iv) fully associative?(8%)
(b)Draw 4 diagrams of the 32-bit address for the above four type of caches and indicate in each diagram which bit fields are used for tags, index to block, block offset, etc., respectively. (8%)
(c)What block number does byte address 1200 map to in the four types of caches, respectively? (4%)

5. (10%) Suppose we have a processor with a base CPI (clock-cycles per instruction) of 1.0, assuming all references hit in the primary cache, and a clock rate of 500 MHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%.
(a)What is the miss penalty to main memory in clock cycles and the effective CPI for this one-level caching processor? (4%)
(b)What will the effective CPI and how much faster will the machine be if we add a secondary cache that has a 10-ns access time for either a hit or a miss and the secondary cache is large enough to reduce the miss rate to main memory to 2%? (6%)

6. (20 points) (a) Explain why most of today's computer systems use *2's complement* instead of *signed-magnitude* in their hardware implementations. (b) Explain the purpose of *jump-and-link (jal)* instruction. (c) Explain why geometric mean may be useful in comparing machine performance. (d) Power of 2 is normally used in the design of a computer. Is it possible to construct a five-way set associative cache? Why? (e) Is MIPS (million instructions per second) an accurate measure for comparing performance of different architecture? Why?

7. (7 points) How will you fill in a personal record such as "Tom Lien" in the following table using little-endian? Assume each row consists of 4 bytes.

8. (8 points) The following figure is a 32-bit ALU constructed from 32 1-bit ALUs. CarryOut of the less significant bit is connected to the CarryIn of the more significant bit. Can you add a simple logic to detect if there is an overflow?