九十二學年度 電機工程學 系（所） 乙 組碩士班研究生招生考試

科目 計算機組織 科號 2403 共 2 頁第 1 頁 *請在試卷【答案卷】內作答

1. (10%) Compute the value of the following floating-point number A based on the IEEE standard. (Note: this floating-point number is composed of three fields, i.e., a sign bit, 8 exponent bits, and 23 significant bits.).

$$A = (11000000101000000000000000000000)$$

2. (10%) Consider the addition process of the following two binary numbers A and B. Determine the so-called *Carry Generate* and *Carry Propagate* signals for each bit.

$$A = (00011010)$$
$$B = (11100101)$$

3. Consider the process of adding up two floating-point numbers in a microprocessor.
   (a) (6%) Derive the proper sequence of the following three operations. (1) *Addition of Significands* (2) *Normalization* (3) *Alignment of Exponents*.
   (b) (6%) What operation is still needed in addition to the above three operations.

4.. (12%) One extension of the MIPS instruction set architecture has two new instructions called `movn` (move if not zero) and `movz` (move if zero). For example, the instruction

```
movn $8, $11, $4
```

copies the contents of register 11 into register 8, provided that the value in register 4 is nonzero (otherwise it does nothing). The `movz` instruction is similar but copying takes place only if the register's value is zero. Show how to use the new instructions to put whichever is larger, register 8's value or register 11's value, into register 10. If the values are equal, copy either into register 10. You may use register 1 as an extra register for temporary use. Do not use any conditional branches.

5. (14%) Consider three machines with different cache configurations:
   Cache 1: Direct-mapped with one-word blocks.
   Cache 2: Direct-mapped with four-word blocks.
   Cache 3: Two-way set associative with four-word blocks.

The following miss rate measurements have been made:
   Cache 1: Instruction miss rate is 4%; data miss rate is 8%.
   Cache 2: Instruction miss rate is 2%; data miss rate is 5%.
   Cache 3: Instruction miss rate is 2%; data miss rate is 4%.

For these machines, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + Block size in words. The CPI for this workload was measured on a machine with cache 1 and was found to be 2.0. Determine which machine is the fastest and which is the slowest.

6. (10%) A program repeatedly performs a three-step process: It reads in a 4-KB block of data from disk, does some processing on the data, and then writes out the result as another 4-KB block elsewhere on the disk. Each block is contiguous and randomly located on a single track on the disk. The disk drive rotates at 7200 RPM, has an average seek time of 8 ms, and has a transfer rate of 20 MB/sec. The controller overhead is 2 ms. No other program is using the disk processor, and there is no overlapping of disk operation with processing. The processing step takes 20 million clock cycles, and the clock rate is 400 MHz. What is the overall speed of the system in blocks processed per second?

7. (10%) Suppose register $s0 has the binary number

   $1111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1111_{two}$

   and that register $s1 has the binary number

   $0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0001_{two}$

   What are the values of registers $t0 and $t1 after these two instructions?

```
slt     $t0, $s0, $s1     # set on less than signed comparison
sltu    $t1, $s0, $s1     # set on less than unsigned comparison
```

8. (10%) Explain [1] spatial locality, [2] write-back cache, [3] page table, [4] compulsory misses, and [5] branch delay slot

9. (12%) Which change is more effective on a certain machine: speeding up 10-fold the floating point square root operation only, which takes up 20% of execution time, or speeding up 2-fold all other floating point operations, which take up 50% of total execution time? Assume that the cost of accomplishing either change is the same, and the two changes are mutually exclusive.