國　立　清　華　大　學　命　題　紙

九十二學年度 電機工程學系甲、乙組暨光電工程研究所 碩士班研究生招生考試

科目 電子學 科號 2303、2402、2503 共 2 頁第 1 頁 *請在試卷【答案卷】內作答

1. The diodes in the circuit are ideal. The resistors are $R_1=R_2=R_3$. The voltage $V_1=10$ V. Determine the voltage V_o for V_2= (a) 10 V, (b) 2 V, (c) –1 V, (d) –10 V and (e) –13 V.
(10% Fig. P1)

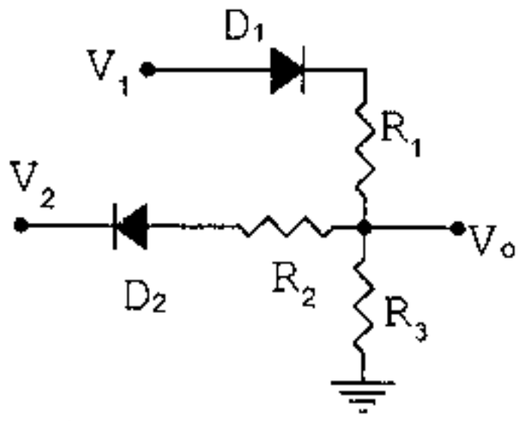

Fig. P1

2. In the voltage regulator as shown, the parameters are $V_{z0}=5.7$ V, $r_z=10\ \Omega$ for the zener diode and $\beta=100$ for the BJT, and $R_1=R_2=1\ k\Omega$. The supply voltage is $V_{PS}=10$ V $\pm 10\%$. The output voltage is $V_0=5$ V $\pm \Delta\%$. Find the value of Δ and the output resistance R_{out}.
(10% Fig. P2)

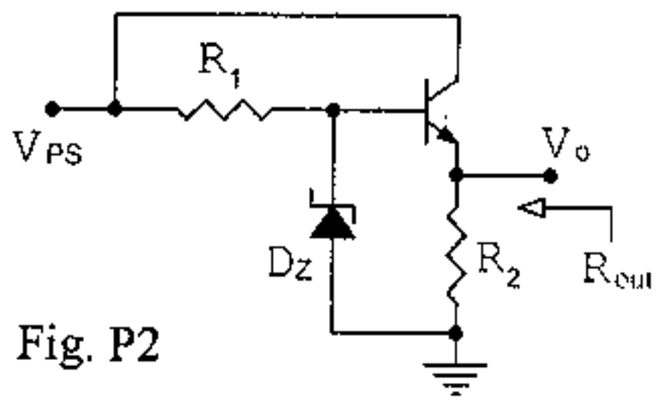

Fig. P2

3. The transistor parameters in the circuit are $\beta=100$, $V_A=100$ V for the BJT; $K_n=1$ mA/V^2, $\lambda=0.02\ V^{-1}$ for the FET. The capacitor $C=\infty$. The voltage V_S and the resistors R_1, R_2, R_3 are designed such that the collector and drain currents are $I_{CQ}=I_{DQ}=1$ mA. Determine the voltage gain V_o/V_i and the output resistance R_{out}.
(15% Fig. P3)

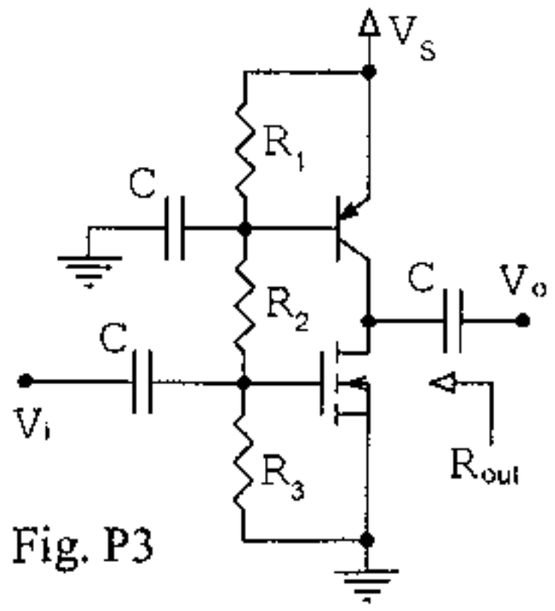

Fig. P3

4. For a single common source device, please derive its unity-current-gain frequency. (draw the small signal model and consider all the parasitic capacitances and output resistance). (10%)

5. Fig. P5 is a differential amplifier with I_{D5}=0.2mA. If all the devices are biased with V_{GS}-Vt = 0.2V, where NMOS and PMOS threshold voltages are Vtn=|Vtp|=0.6V. NMOS Early voltage is V_An=10V and PMOS is V_Ap=20V. R_1=R_2=10K, C_1=C_2=C_3=C_4=1pF. Neglect the body effect.
Please
(a) draw the differential mode half circuit and calculate its differential mode gain. (5%)
(b) draw the common mode half circuit and calculate its common mode gain. (5%)
(c) draw the different mode frequency response. (5%)
(d) what do R_1 and R_2 do for differential and common mode operation in this circuit? (5%)

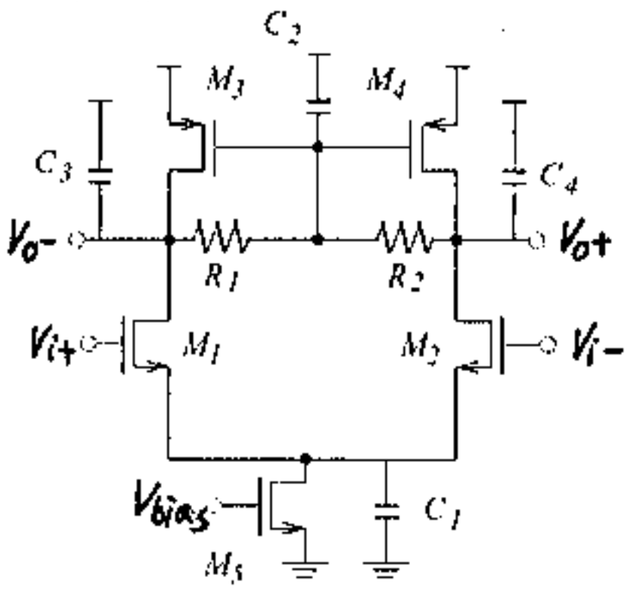

Fig. P5

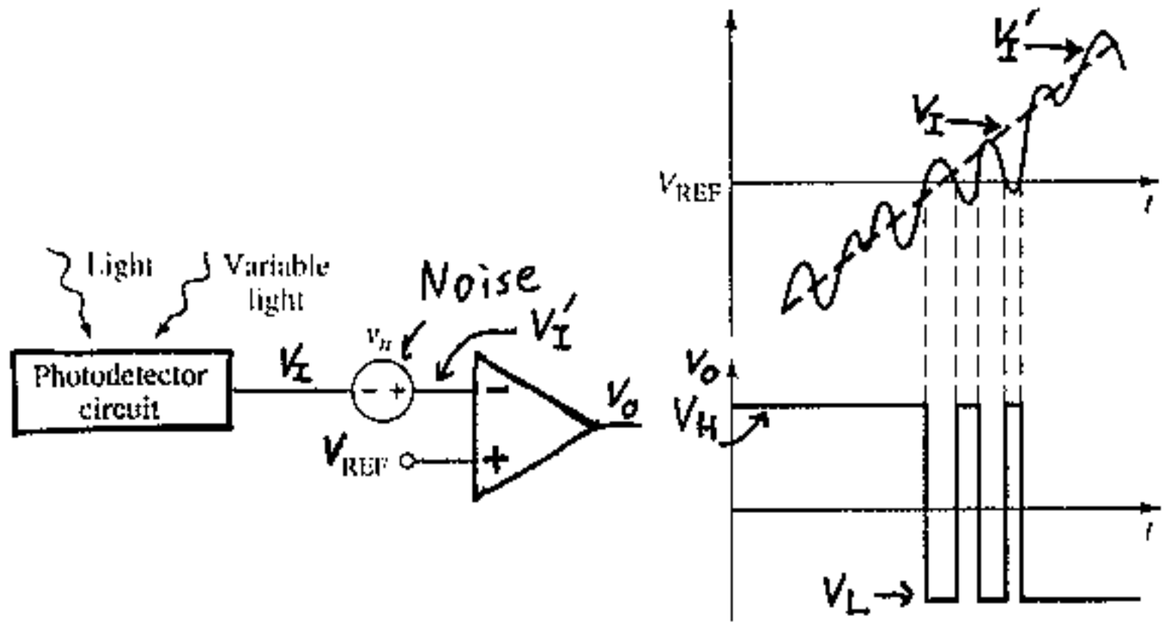

Fig. P6

6. As shown in Fig. P6, a street light system is unstable when noise exists around the threshold. Please redesign this system by using Schmitt trigger.
(a) Show your design with simple explanation. (10%)
(b) If the output of the OP is V_H or V_L (Saturation Voltages with $V_H > 0 > V_L$), find the threshold voltages in your design. (10%)

7. (15%) This is the problem about conventional Dynamic Random Access Memory (DRAM).
(a) Draw the structure of a conventional DRAM cell.
(b) How to perform the read operation? (Note that the bus capacitance is greater than that in DRAM cell)
(c) If a constant leakage current I_{leak} exists, and the capacitance of the DRAM cell is C_{cell}, calculate the refresh period if the power supply and threshold voltage of the NMOS pass transistor is V_{DD} and V_{TN}, respectively. (Logic-1 $\geq V_{DD}/2$)