1. (10%) Define the following terminology briefly.
   (1) CPI
   (2) Performance metric MFLOPS
   (3) Microprogramming
   (4) VLIW
   (5) Superscaler

2. (15%) A computer with immediate/constant instruction set has the following machine code:

Operand 6-bit	Register Source 5-bit	Register Destination 5-bit	Immediate 16-bit

   Answer the questions below:
   (a) At most how many registers does this computer have? (3%)
   (b) At most how many operations in this format does this computer have? (4%)
   (c) What is the largest positive number in 2's complement form in Immediate field of this format? (4%)
   (d) What is the most negative number in 2's complement form in Immediate field of this format? (4%)

3. (15%) An arithmetic operation called "?" has the following functions:
   Input a_i, b_i, c_i,
   Output s_i, c_{i+1};
   $s_i = a_i \oplus b_i \oplus c_i$, where $\oplus$ means exclusive-or.
   $c_{i+1} = c_i b_i' + a_i c_i + a_i b_i'$, where x' means the complement of x.
   Answer the following questions:
   (a) If i = 4 (4 bits) with data $c_0 = 0$, $A = (a_3\ a_2\ a_1\ a_0) = (0010)$ and $B = (b_3\ b_2\ b_1\ b_0) = (0111)$, find the answer $S = (s_3\ s_2\ s_1\ s_0) = ?$ (7%)
   (b) What is this operation? (In other words, find "?") (8%)

4. (15%) In a microprocessor, the instructions are divided into five classes: ALU, LOAD, STORE, BRANCH, and JUMP.
   (1) For each type of instruction, indicate in the following Table what operations would be executed: instruction memory access, register file read, ALU operation, data memory access, and register file write. For example, JUMP only needs to perform instruction access but not others. (5%)
   (2) Assume that the delays for the five operations are: instruction memory access (2ns), register file read (1ns), ALU operation (2ns), data memory access (2ns), register file write (1ns). Calculate the clock cycle time if single-cycle architecture is adopted. (5%)
   (3) Assume the following instruction mix: 25% loads, 10% stores, 45% ALU instructions, 15% branches, and 5% jumps. If a perfect variable-length clock were achievable, what would be the average clock cycle time? (5%) (Hint: variable-length clocking scheme means that the clock cycle time can dynamically adjusted according to the type of the instruction under execution).

operations / instruction class	instruction memory access	register file read	ALU operation	data memory access	register file write
ALU					
Load					
Store					
Branch					
Jump	yes	no	no	no	no

(請將此表重畫於試卷上,並填上答案。)

5. (15%) The data-path of a microprocessor is decomposed into five pipeline stages:

IF: instruction fetch

ID: instruction decode and register file read

EX: execution or address calculation

MEM: data memory access

WB: write back to register file

Consider the instruction sequence given.

(a) Show all data hazards in this instruction sequence. (Note: instruction format is: <OP-code> <destination-register> <source-register1> <source-register2>. (5%)

(b) Convert the above sequence into a hazard-free one by properly inserting *nop* instructions. Show the final sequence. (5%)

(c) Use the forwarding technique to minimize the number of pipeline stalls. Show every data-forwarding path. (5%)

Instruction sequence			
Sub	$2,	$1,	$3
And	$4,	$2,	$5
Or	$4,	$4,	$2
Add	$9,	$4,	$2

6. (16%) You have been given 18 32K x 8-bit SRAMs and some logics necessary to build an instruction cache for a processor with 32-bit address and 32-bit data word.

(a) What is the largest size (i.e., the largest size of data storage area in bytes) direct-mapped instruction cache that you can build with one-word (32-bit) blocks using the given SRAM chips? (3%)

(b) Draw a block diagram of the instruction cache of your design. The block diagram should show the breakdown of the address into its cache access components. It should also clearly display the important ingredient of a cache system, e.g., tag address, block address, byte offset, valid bit, tag bits, data bits, cache hit generation, and the wires connecting them. (8%)

(c) What's the number of total tag bits in the above design? (3%)

(d) If two-way set associative cache is to be designed in this case, what's the largest size instruction cache that you can build with one-word blocks using the given SRAM chips? (3%)

(Hint: you may not need all of them.)

7. (8%) Consider the following computer system:

- A CPU that sustains 300 million instructions per second and averages 50,000 instructions in the operating system per I/O operation.
- A memory backplane bus capable of sustaining a transfer rate of 100 MB/sec.
- SCSI-2 controllers with a transfer rate of 20 MB/sec and accommodating up to seven disks.
- Disk drives with a read/write bandwidth of 5 MB/sec and an average seek plus rotational latency of 10 ms.

If the workload consists of 64-KB reads (where the block is sequential on a track) and the user program needs 100,000 instructions per I/O operation, find (a) (4%)the maximum sustainable I/O rate and (b) (4%) the number of disks and SCSI controllers required. Assume that the reads can always be done on an idle disk if one exists (i.e., ignore disk conflicts).

8. (6%) Suppose we have a system with the following characteristics

- A memory and bus system supporting block access of 4 to 16 3-bit words.
- A 64-bit synchronous bus clocked at 200 MHz, with each 64bit transfer taking 1 clock cycle, and 1 clock cycle required to send an address to memory
- Two clock cycles needed between each bus operation. (Assume the bus is idle before an access.)
- A memory access time for the first four words of 200 ns; each additional set of four words can be read in 20 ns. Assume that a bus transfer of the most recently read data and a read of the next four words can be overlapped.

(a) Find the sustained bandwidth and the latency for a read of 256 words for transfers that use 4-word blocks and for transfers that use 16-word blocks. (4%)

(b) Compute the effective number of bus transactions per second for each case. (2%)

Recall that a single bus transaction consists of an address transmission followed by data.