八十八學年度 電機工程 系(所) 乙 組碩士班研究生招生考試

科目 計算機組織 科號 4504 共 4 頁第 1 頁 *請在試卷【答案卷】內作答

1. (10%)

Fill in the following blanks

(a) In multi-processing environment, each process is in one of the following three states:

_____, _____, _____.

(b) Assume a program A is executing and requesting an input line from the keyboard, it will call the I/O service routine and then it will be changed from the _____state to _____state.

(c) At this moment, the Operating System(OS) will select another program B in ____state, and perform a _____ process that saves the context of program A (from CPU) and loads the context of program B (to CPU).

(d) Therefore, program B can be changed to ____state.

(e) After the original I/O operation (request from program A) has been finished, then OS will change the status of program A from ____state to ____state.

2. (15%)

There are two kinds of adders: (1) ripple-carry adder (2) carry-look-ahead adder. Please answer the following questions:

(a) For an 16-bit addition, if we use ripple adder and assume that delay from c_i to c_{i+1} of any full adder is 1-nsec, then the 16-bit addition takes _____nsec.

(b) If we use carry-look ahead adder, the 16-bit adder is divided into four 4-bit adders, In each 4-bit adder there is a 4-bit carry-look circuit. Assume that there is one gate delay for all G_i and P_i and two gate delays for each carry c_4, c_8, c_{12}, c_{16} and final three delay for s_{15} . How many gate delays is required for generating c_{16} after X, Y, and c_0 are applied as input ?

(c) Assume that each gate delay requires 0.5nsec. This 16-bit adder requires _____nsec for a single addition operation. Another faster way to apply look-ahead circuit is to add a second-level look-ahead circuit.

(d) Please ***draw a diagram*** to illustrate how the second-level look-ahead circuit is added ?

(e) With second-level look-ahead circuit, how many gate delay is required for generating c_{16} after X, Y, and c_0 are applied as input ?

(f) Assume that each gate delay requires 0.5nsec. This 16-bit adder requires _____ nsec for a single addition operation.

3. (15%)

A 2M-byte RAM is to be designed from 256K×4-bit RAM ICs. Assume that 1-out-of-4 decoder ICs and ICs containing standard logic gates are available. The main design goal is to minimize the number of ICs used.

(a) Carry out the design and give its block diagram assuming that each RAM chip has a single chip-enable line CE. (8%)

(b) Repeat the design assuming that each RAM chip has two chip-enable lines CE_1 and CE_2, and is enabled if and only if $CE_1 = CE_2 = 1$. (7%)

4. (10%)

(a) Convert the decimal number –13.6 to 8-bit 2's-complement binary number representation, assuming that we have a 2-bit fraction. (5%)

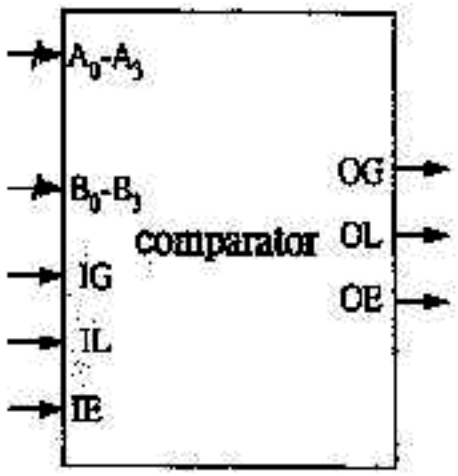
(b) In general, a floating-point number system can represent a larger range of numbers than a fixed-point one, given the same word length. Do the floating-point numbers also have higher precision than the corresponding fixed-point ones? Explain. (5%)

5. (10%) If you only have the 2-to-1 multiplexers, can you use these multiplexers as the basic building block to construct an 8-to-1 multiplexer without using any other logic gates.

6. (15%) A 4-bit comparator with specification is shown as following figure and table, where x means don't care term:

(a) Can you use four 4-bit comparators to compare two positive binary numbers of 16-bit each? (A_{n-1} MSB, A_0 LSB)

(b) How about use six 4-bit comparators to compare two positive binary numbers of 25-bit each?



A and B	IG	IL	IE	OG	OL	OE
A>B	0 1	0 1	x x	1	0	0
A=B	0 1	0 1	x x	0	0	1
A<B	0 1	0 1	x x	0	1	0
x	1	0	0	1	0	0
x	0	1	0	0	1	0
x	0	0	1	0	0	1
Other cases				Un- predictable		

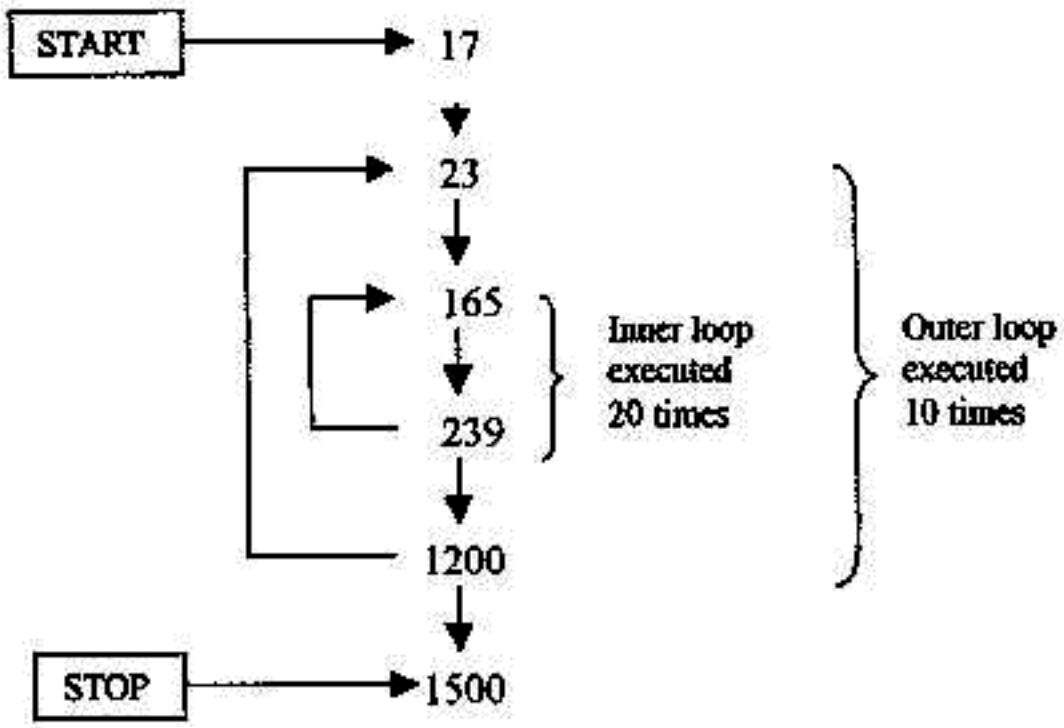
7. (15%)
A program consists of two nested loops – a small inner loop and a much larger outer loop. The general structure of the program is given in the following figure. The decimal memory addresses shown delineate the location of the two loops and the beginning and end of the total program. All memory locations in the various sections, 17-22, 23-164, 165-239, and so on, contain instructions to be executed in straight-line sequencing. The program is to be run on a computer that has an instruction cache organized in the direct-mapped manner and that has the following parameters:

Main memory size	64K words
Cache size	1K words
Block size	128 words

The cycle time of the main memory is 10τ s, and the cycle time of the cache is 1τ s.

(a) Specify the number of bits in the TAG, BLOCK, and WORD fields in main memory addresses. (5%)

(b) Compute the total time needed for instruction fetching during execution of the program. (10%)



8. (10%)
Pipelining is often used to increase the instruction throughput in processor design. In general, an n-stage pipeline has the potential to increase throughput n times, compared to non-pipelined operation. However, the increase in throughput is limited by delay incurred when the pipeline is stalled.

(a) List three situations in which the pipeline will be stalled.

(b) A pipeline processor uses the delayed branch technique. You are asked to recommend one of two possibilities for the design of this processor. In the first possibility, the processor has a four-stage pipeline and one delay slot, and in the second possibility, it has a six-stage pipeline with two delay slots. Compare the performance of these two alternatives by calculating their throughput improvements over non-pipelined architecture, taking only the branch penalty into account. Assume that 20 percent of the instructions are branch instructions and that an optimizing compiler has an 80 percent success rate in filling the single delay slot. For the second alternative, the compiler is able to fill the second delay slot 25 percent of the time.