八十六學年度 電机工程學系(所) 乙 組碩士班研究生入學考試

科目 計算機組織 科號 3104 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. Consider a cache (M_1) and main memory (M_2) hierarchy with the following characteristics:

M_1: 16K words, 50ns access time
M_2: 1M words, 100ns access time

Assume eight-word cache blocks and a set size of 256 words with set-associative mapping.

(a) Show the mapping between M_1 and M_2. (5%)

(b) Calculate the effective memory-access time with a cache bit ratio of 0.95. (5%)

2. Design a sequential circuit that multiplies an unsigned binary number N of arbitrary length by 3. N is entered serially via input line x with its least significant bit first. The result representing $3N$ emerges serially from the circuit's output line z. Construct a state table for your circuit and give a complete logic circuit that uses JK flip-flops and NAND gates only. (15%)

3. How do you construct an n-bit adder and an $(n-1)$-bit adder in parallel by using a $2n$-bit adder with overflow detection and a minimum number of extra gates? Note that both the n-bit and $(n-1)$-bit adders also have the overflow detection function. (15%)

4. Find the error(s) in the following operations and explain: (8%)

In 2's-complement representation, we have

$$-2.75_{10} + 3.625_{10} = (101.01)_2 + (011.101)_2 = (0.111)_2 = 0.875_{10},$$

but in 1's-complement representation, we have

$$-2.75_{10} + 3.625_{10} = (101.00)_2 + (011.101)_2 = (0.101)_2 = 0.675_{10}.$$

5. Consider a 1K×4 RAM which is to be redesigned and protected by the Hamming code. Let the 4-bit data be $M = M_3M_2M_1M_0$.

(a) How many check bits are required? (3%)

(b) If the number of check bits is k, i.e., the check bits are $C = C_{k-1}C_{k-2}\cdots C_1C_0$, and the code word to be written into the RAM is $W = W_{k+3}\cdots W_1W_0$, what are the positions of the respective bits of M and C in W? That is, give the mapping from $\{M_3, M_2, M_1, M_0, C_{k-1}, \cdots, C_1, C_0\}$ to $\{W_{k+3}, \cdots, W_1, W_0\}$. (3%)

(c) How do you generate the check bits? (3%)

(d) Give the block diagram of the Hamming coded RAM. Label the widths of the interconnections between modules. (6%)

6. The W&W Computer and Pizza Company is planning to introduce a new series of scientific computers covering a wide range of cost and performance. Give the arguments for and against using microprogrammed control in the CPUs of the various models of the series (7%)

7. Answer the following questions: (15%)

(a) Is the interrupt break point (i.e., where the CPU respond to the interrupt request) at the instruction cycle or the CPU clock cycle?

(b) Is the DMA break point (i.e., where the CPU respond to the DMA request) at the instruction cycle or the CPU clock cycle?

(c) Explain the following three bus arbitration methods: (i) daisy chain; (ii) polling; (iii) independent requesting.

(d) Compare the three methods in (c) in terms of (i) system simplicity; (ii) number of control lines; (iii) system reliability (e.g., what if one I/O device has error?); and (iv) system flexibility (e.g., what if we want to add more I/O device to the system?).

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4. A carry look ahead can be extended to handle *mk* bits by performing carry-lookahead addition on *m* groups of *k* adjacent bits and transferring the output carry bit of each group to the carry input of its left neighbor. Assume in this kind of adder, each group can generate an output carry *d* time units (*d* is the two-level delay) after it receives its input carry. Please use and complete the following diagram to

(1) Design a 16-bit adder (*k=4 and m= 4*) and let each group be a 4-bit carry look ahead adder, and there is ripple carry between groups.

(2) Design the same adder using another carry look ahead circuit above the four groups.

(3) Compute and explain the total delay time (how many *d* ?) of the above two kinds of 16-bit adders. (15%)