國立清華大學命題紙

八十五學年度 電機/電子 系（所） 丙 組碩士班研究生入學考試

科目 固態電子元件 科號 3105 共 2 頁第 1 頁 *請在試卷【答案卷】內作答

(1) Calculate the position of the Fermi level from the intrinsic Fermi level E_i in equilibrium in each of the following situations. Assume the material is silicon at room temperature and $n_i = 1\times10^{10} cm^{-3}$. ($Log_{10}2 = 0.301$ and $Log_{10}3 = 0.477$)

(a) $N_D = 1\times10^{17} cm^{-3}$ and $N_A = 1\times10^{16} cm^{-3}$. (5%)

(b) $N_D = 1\times10^{17} cm^{-3}$, $N_A = 1\times10^{16} cm^{-3}$, and a deep acceptor located at E_i with $N_{A_{Deep}} = 5\times10^{16} cm^{-3}$. (5%)

(c) $N_A = 1\times10^{17} cm^{-3}$ with a deep donor located at 0.25 E_G from conduction band edge E_C with $N_{D_{Deep}} = 5\times10^{16} cm^{-3}$,and a deep acceptor located at E_i with $N_{A_{Deep}} = 1\times10^{16} cm^{-3}$. (5%)

(2) A N-type silicon sample ($N_D = 1\times10^{16} cm^{-3}$) contains $N_T = 1\times10^{15} cm^{-3}$ generation/recombination centers located at the intrinsic Fermi level E_i with carrier capture cross section $\sigma_n = \sigma_p = 1\times10^{-15} cm^{-2}$. Assume the thermal velocity of carrier is $v_{thn} = v_{thp} = 1\times10^{7} cm/\sec$.

(a) Calculate the generation rate if the region is depleted of mobile carriers. (5%)

(b) Calculate the generation rate in a region where only the minority-carrier concentration has been reduced appreciably from its equilibrium value. (5%)

3. (a)Explain the origin of Zener breakdown and avalanche breakdown.
(b)Based on(a), discuss which of these two breakdown mechanisms will be enhanced if the doping levels of the semiconductor increase.
(c)Based on(a), discuss which of these two breakdown mechanisms will be enhanced if temperature increases.(15%)

4. Supposed you are given two diodes, one with PN junction and the other with Schottky junction, and you are allowed only to measure the I-V (current-voltage) at various temperatures; discuss how to distinguish the Schottky diode from the PN diode.(10%)

5.(a)In integrated circuits, a transistor may be connected as a diode. Sketch five possible diode configurations along with the minority-carrier distribution in the base for npn transistor.(10%)
(b)Use the doping profile and carrier distribution to compare the diode performance in speed, conductance, and breakdown voltage if the impurity profile of the double-diffused transistor is assumed.(5%)

6.A n-channel JFET has the following data at 300K: $N_A = 10^{19} cm^{-3}$, $N_D = 8 \times 10^{15} cm^{-3}$, the metallurgical channel thickness a is $0.75\,\mu m$, and the channel length L is $20\,\mu m$. Qualitatively predict what happens to (1) internal pinchoff voltage V_{po}, (2)drain-to-source current I_{DS}, and (3)transconductance, gm, if
(a) N_D is increased.
(b) a is decreased.
(c) L is decreased.(10%)

7.(a)Plot the cross-sectional view of a p-well CMOS structure and explain how does latch-up phenomenon occur.(9%)
(b)List three methods that can prevent latch-up.(6%)

8.The experimental C-V_G curve shown below was observed under the following conditions : The d.c. bias was changed very slowly from point (1) to point (2). At point (2) the V_G sweep rate was increaed substantially. Upon arriving at point (3) the sweep was stopped and the capacitance decayed to point (4). Qualitatively explain the observed characteristic.(10%)