八十五學年度 電機工程學 系(所) 乙 組碩士班研究生入學考試

科目 電子學 科號 3002 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. For the high-input-resistance metering circuit of Fig. 1 using a 1-mA meter movement,

5% (a) find the value of the resistor R such that full-scale reading is obtained for v_1= 2.5V.

5% (b) If the meter resistor is 50Ω, what is the OP amp output voltage at half scale?

2. Sketch the transfer characteristic v_o verse v_i for the limiter circuits shown in Fig. 2

All diodes begin conducting at a forward voltage drop of 0.5V and display voltages drops of 0.7V when fully conducting. (10 %)

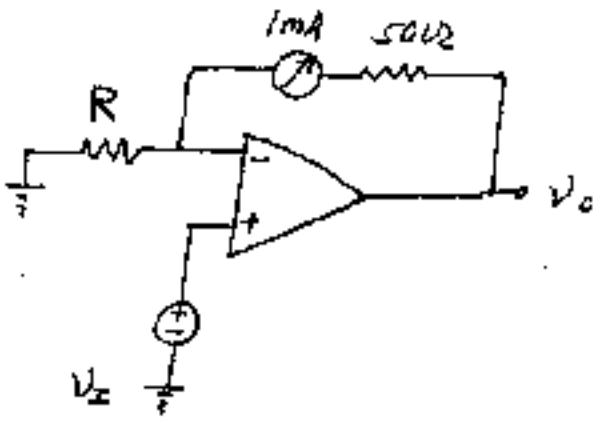


Fig. 1

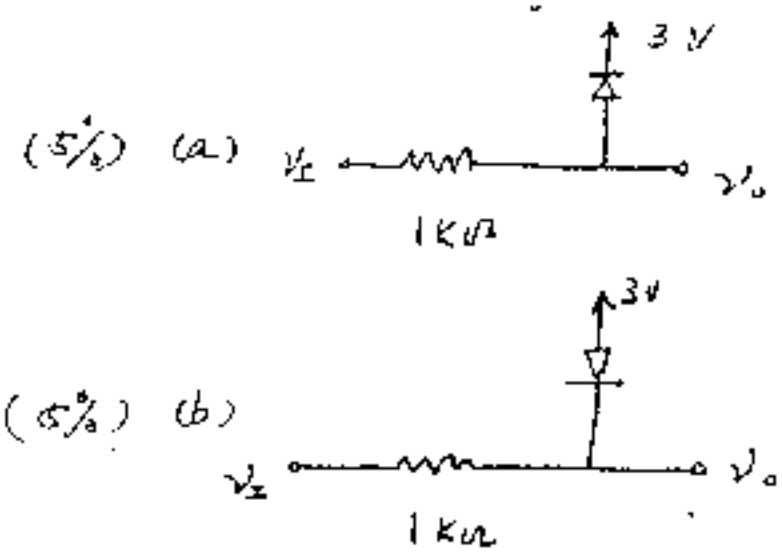
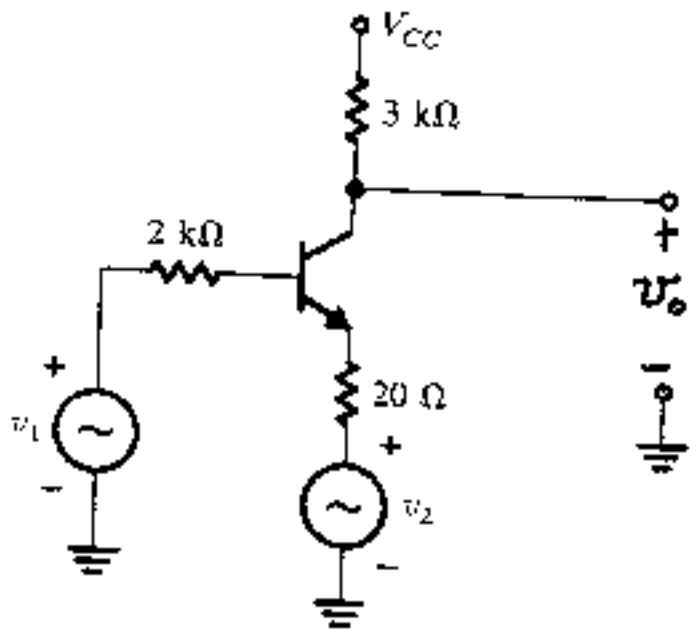
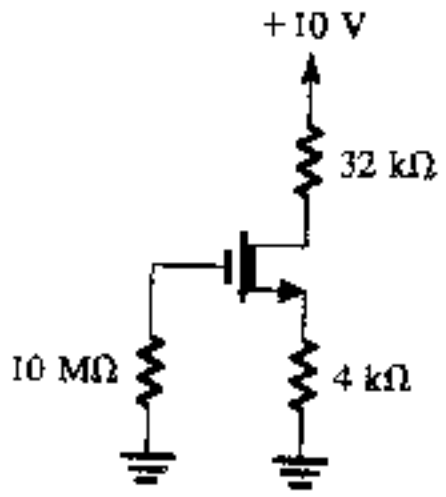


Fig. 2

3. For the following circuit, find v_o in terms of v_1 and v_2. The BJT has β = 100, r_π= 1kΩ, or r_e= 10Ω (12%).



4. Analyze the following to determine I_D and V_D. The depletion MOSFET has V_t = -1v and K= 0.5 mA/V^2 (8%).



5. A circuit as shown in figure 5 consists of an ideal operational amplifier A, two resistors R_1 and R_2, and an input signal source v_I. Assuming that the operational amplifier is powered by $\pm V_m$ and its output voltage limits are 1V short of the power rail voltages.

(a) Analyze the circuit behaviors, and plot the voltage transfer characteristics (v_o versus v_I), indicate all the voltages intersecting both v_o and v_I axes in terms of V_m, R_1, and R_2. (8%)

(b) From the results obtained in part (a), can you identify and give the common well-known name of the circuit? (2%)

(c) In your analysis in part (a), can you use the virtual ground concept which is often employed in analyzing circuits that contain operational amplifiers? Your answer must give supporting reasoning. (4%)

(d) If the circuit is intended to be used as a waveform shaping circuit, that is to shape a sinusoidal wave of $v_I = A_m \sin \omega t$ into a square wave at output v_o with an amplitude of B_m, what is the maximum of B_m? And what is the design constrainton the relation among the parameters B_m, R_1, R_2, and A_m? (6%)

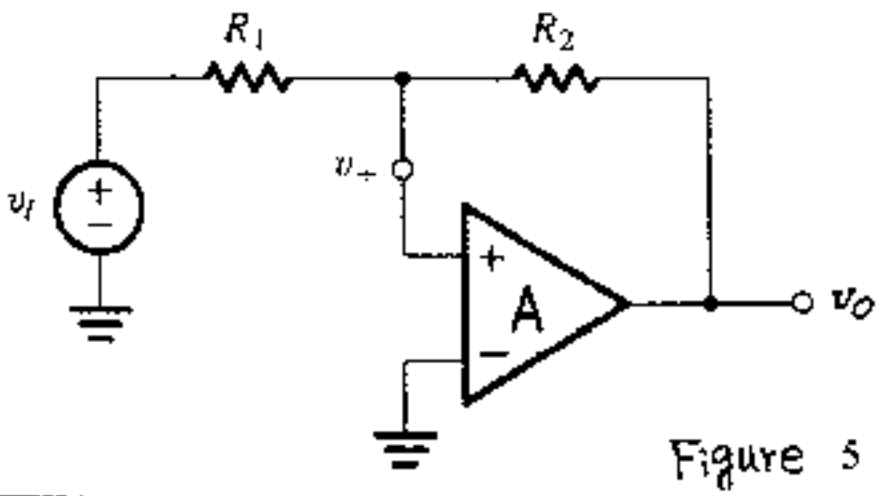
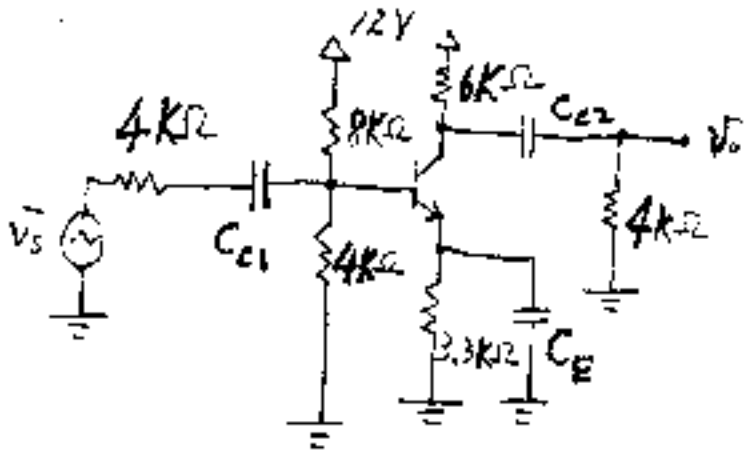


Figure 5

6. Explain why an emitter resistor can effectively increase the output resistance of a common-emitter amplifier. Please also find the enlargement factor for this effect. (10%)

7. Estimate the high-band corner frequency ω_H for the following circuit. Assume that $\beta = 100$ and $c_x = 10c_\mu = 1$ pF. (10%)



8. Compare the inverters implemented in CMOS, depletion NMOS load (Dep.-NMOS), and Enhancement NMOS (Enh-NMOS) load with "equal" dimensions.

9% (a) Fill the blanks with simple comments or with correct connections and

11% (b) draw the voltage transfer characteristics of those 3 inverters, mark V_{OH}, V_{OL}, V_{IH}, V_{IL} at each curve.

(a)	CMOS Inverter	Dep.-NMOS	Enh.-NMOS
Power Dissipations			
Draw connections (include substrate)