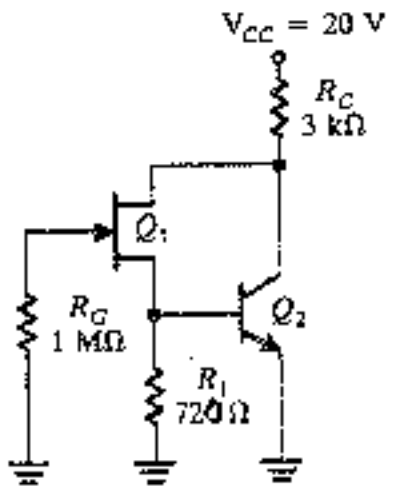
國 立 清 華 大 學 命 題 紙

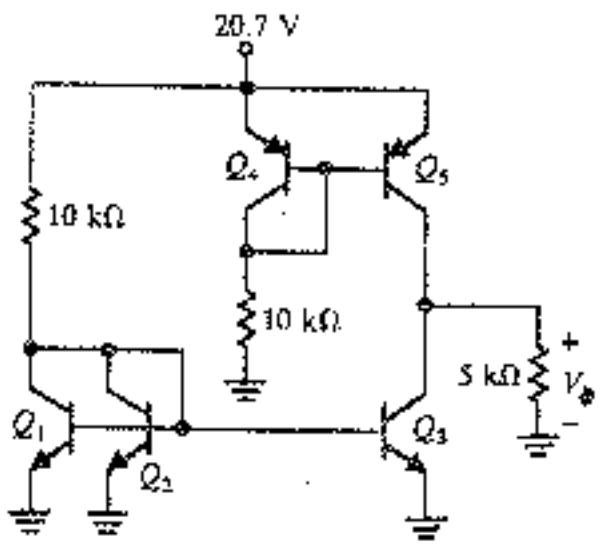
八十四學年度 電機工程研究所 乙 組碩士班研究生入學考試

科目 電子學 科號 2302 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. In the following circuit, Q1 has I_{DSS} = 4 mA and V_P = -1.4 V and Q2 is silicon with β = 100 and V_{BE2} = 0.7 V. Find the dc V_{GSQ}, I_{DQ}, I_{B2}, I_{C2}, and V_{CE2}. (10%)

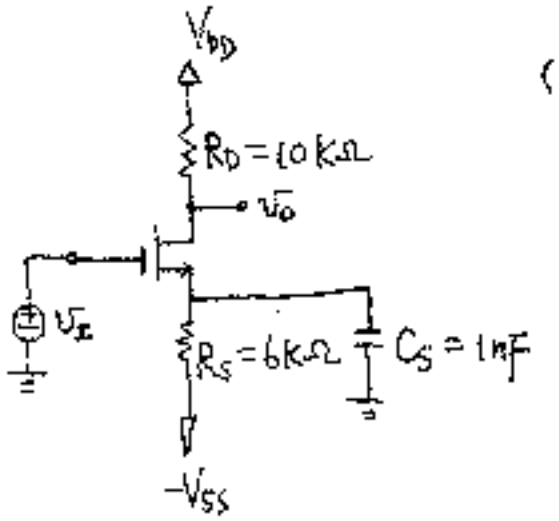


2. Find the dc voltage Vo for the following circuit. (10%)
($|V_{BE}|$ = 0.7V)



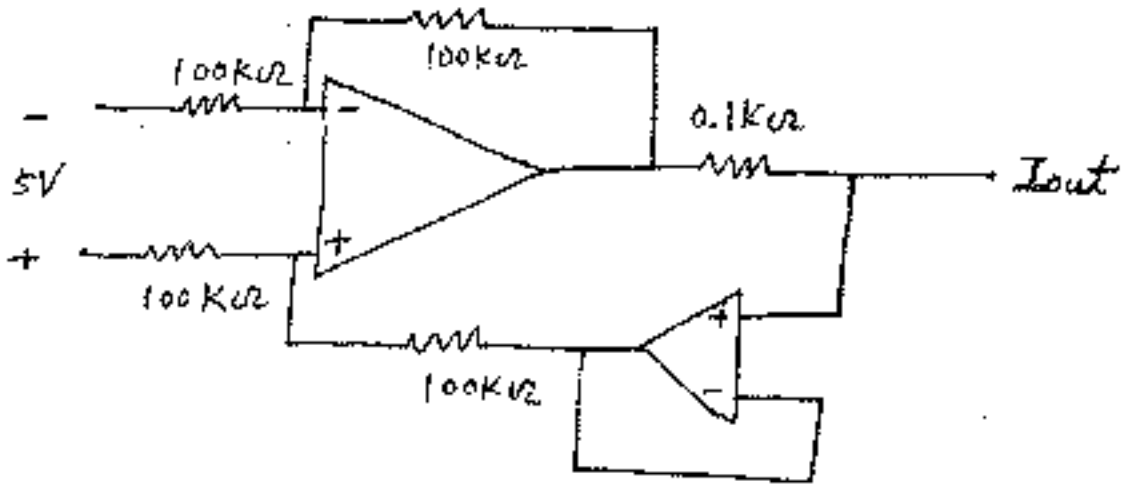
3. A capacitively coupled amplifier has a midband gain of 100 and two poles at 10 kHz and 100 Hz, respectively. To improve the immunity of the amplifier to the gain variation due to environmental parameter change, negative feedback is used to obtain a desensitivity factor of 20dB. What are the midband gain, the upper 3-dB frequency and the lower 3-dB frequency of the feedback amplifier? (10%)

4. Find the midband gain and the lower corner frequency for the common-source FET amplifier shown in the figure. (10%)



($I_D = 1\,mA$, $g_m = 1\,m\mho$)

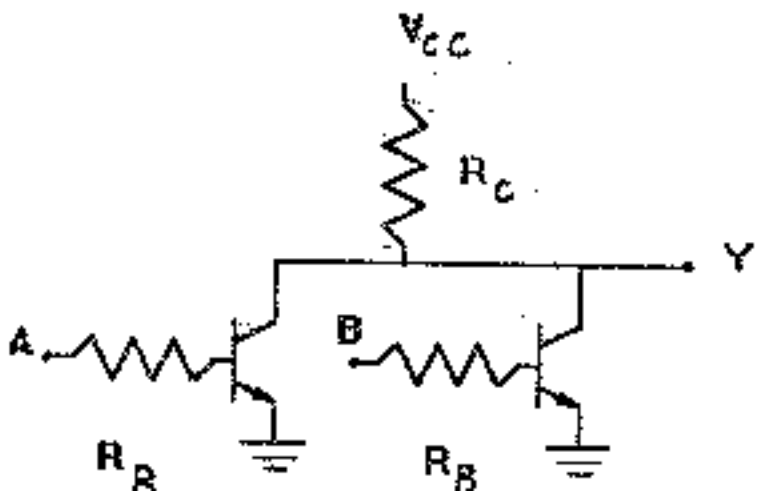
5. In the following current source, please find out what I_{out} is. Both Op Amps are assumed to be ideal. (20%).



6. (10%) For a two-input RTL gate as shown below, when driving N identical gates, answer the following questions.

(a) Find the logic function of this RTL gate, i.e., Y = ?.

(b) Let V_{BE} = 0.7 V, V_{CC}=5V, find V_{OH} in terms of N, R_C, and R_B.



7. (10%) For a logic inverter with output levels of V_{OL} and V_{OH}, a power supply V_{DD}, input switching frequency f cycles/second, and a load capacitance C_L, find the dynamic power dissipation.

8. For the circuit shown below with the relative EBJ area indicated, what are (a) the value of i_o (expressed in terms of V_{ref} and R_{ref}) and (b) the range of i_o? (20%)