類組：電機類　科目：計算機系統(計算機組織)(300A)　※請在答案卷內作答

一. [12%] Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 2, 4, and 2 respectively. Also assume that the instruction mix is 40%, 20% and 40% for the three kinds of instructions respectively. Assume each processor has a 3 GHz clock frequency.

(1) [4%] Assume the clock frequency of this processor is proportional to its supply voltage. If we add an extra processor to this system but reduce the supply voltage from 1.8V to 1.2V, what is the performance improvement of this change? Assume only clock frequency is affected by this change and the program can be perfectly parallelized on multiple processors.

(2) [4%] In (1), if the CPI of the arithmetic instructions is doubled when the clock frequency is slowed down, what is the performance improvement of this dual-core system?

(3) [4%] One way to evaluate the efficiency of a processor is using the power-delay product (PDP). Smaller PDP means better efficiency. In this problem, we define the PDP as the product of power and cycle time. Assume the power consumption of this processor is proportional to the square of its supply voltage. Can we obtain efficiency improvement in terms of PDP in (1)? Please briefly explain your reason.

二. [8%] Consider the following MIPS code sequence:

```
LOOP: slt $t2, $0, $t1
      beq $t2, $0, DONE
      subi $t1, $t1, 1
      addi $s2, $s2, 2
      j LOOP
DONE:
```

(1) [4%] Assume that the register `$t1` is initialized to the value of 10. What is the value in register `$s2` assuming `$s2` is initially zero?

(2) [4%] Assume that the register `$t1` is initialized to the value of *N*. How many instructions are executed?

三. [7%] MIPS instructions:

(1) [3%] In MIPS, there are instructions `lb`, `lbu`, and `sb` for load byte, load byte unsigned, and store byte, respectively; however, there is no the following instruction `sbu`. Why not?

(2) [4%] A MIPS branch instruction performs a modification of PC+4 if the condition is true. Suppose that the maximum range of the jump in MIPS is PC-*A* to PC+*B*, where both *A* and *B* are positive numbers. What are *A* and *B*?

四. [10%] IEEE 754-2008, the IEEE standard for floating-point (FP) arithmetic, contains a half precision that is only 16 bits wide, in which the left most bit is the sign bit followed by the 5-bit exponent with a bias of 15 and the 10-bit mantissa. A hidden 1 is assumed.

(1) [2%] Explain why the biased exponent is generally applied to the FP representation?

(2) [8%] Please write down the bit pattern to represent 1.5625×10^{-1} using IEEE 754-2008. Comment on how the ***range*** and ***accuracy*** of this 16-bit FP format compares to the single precision IEEE 754 standard.

注意:背面有試題

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五. [10%] Suppose that you have a computer that, on average, exhibits the following characteristics on the programs you run:

Type	Distribution	IF	ID	EX	MEM	WB
Load	25%	2ns	1ns	3ns	3ns	1ns
Store	10%	2ns	1ns	3ns	2ns	X
Arithmetic	45%	2ns	1ns	3ns	X	1ns
Branch	20%	2ns	1ns	3ns	X	X

i. IF: instruction fetch; ID: instruction decode; EX: ALU execution; MEM: data memory access; WB: write back

ii. X denotes that the corresponding stage is not needed

(1) [4%] If your computer is implemented as a single-cycle processor, what is its throughput (measured by "instructions per second")?

(2) [4%] If your computer is implemented as a multi-cycle processor, in which each stage is executed in one cycle, what is its throughput (measured by "instructions per second")?

(3) [2%] If your computer is implemented as a 5-stage pipelined processor, what is its idealized throughput, assuming that the there are no hazards between instructions?

六. [10%] A RISC processor with 18-stage pipeline runs a program *P* having 6,114 instructions. Branches comprise 23% of the instructions, and the "branch not taken" assumption holds for static branch prediction. Further assume that 40% of the branches are predicted correctly, and there is an average penalty of 1.7 cycles for each mispredicted branch. Additionally, 2% of the total instructions incur an average of 1.3 stalls each. Please calculate the CPI of *P* on this pipeline.

SHOW ALL WORK TO GET FULL CREDIT IF YOUR ANSWER IS CORRECT, PARTIAL CREDIT IF NOT.

七. [25%] Consider a lite version of MIPS (Lite-MIPS) in which the immediate fields in `lw` and `sw` instructions must be zero. Thus, `lw $t0,0($sp)` is legal in Lite-MIPS, but `lw $t0,4($sp)` is not. Lite-MIPS can be implemented with a 4-stage pipeline: IF, ID, EM, WB where the EM stage performs the EX and MEM tasks for the normal 5-stage pipeline in parallel. (Note that no instruction in Lite-MIPS uses both EX and MEM stages.)

(1) [5%] Consider the instruction sequence:

```
lw $t0,0($a0)
sw $t0,0($a0)
```

Fill in the pipeline diagram below to indicate stalls (if any, please mark it with "*") to resolve *data hazards* in the above sequence on the 4-stage pipeline with *full forwarding*.

Clock-cycle / Instruction	1	2	3	4	5	6	7	8
lw								
sw								

注意:背面有試題

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(2) [5%] If the `sw` instruction was replaced with a conditional branch instruction, under what circumstances would a stall be necessary between the two instructions?

(3) [5%] If the `sw` instruction was replaced with `addi $t0,$t0,1` and there was no *forwarding* implemented, how many stalls would be necessary?

(4) [10%] If conditional branch targets are computed in the ID stage, and conditional branch decisions are resolved in the EM stage, what would be the best prediction strategy (never predict, always predict taken, always predict not-taken) for this datapath? Draw pipeline diagrams to support your answer.

八. [18%] Given a four-way set associative cache of 1024 blocks, a 16-byte block size, and a 32-bit address. Assume the access time of this cache is 1ns including all delay, and the average access time of the main memory is 5ns per byte, including all the miss handling.

(1) [2%] What are the numbers of bits for the tag, and index in this cache?

(2) [4%] Below is a list of 32-bit memory address references, given as word addresses. Please identify whether each reference is a hit or miss, assuming the cache is initially empty.
→ 3, 188, 43, 1026, 191, 1064, 2, 40

(3) [5%] Suppose the miss rate at the primary cache is 4%. How much reduction can we obtain on the AMAT if we add a secondary cache that has a 5ns access time and is large enough to reduce the miss rate to 1%?

(4) [2%] Suppose the space of this memory system is extended from 32-bit to 36-bit by using the virtual memory technique, in which each page has 8KB. What are the numbers of bits for the virtual page number and the page offset?

(5) [5%] Assume the TLB is put into the primary cache, and the page table is put into the main memory. What is the AMAT if TLB and cache are both hit? What is the AMAT if TLB is a miss without page fault, assuming the cache is still hit?