國立清華大學 106 學年度碩士班考試入學試題

系所班組別：資訊系統與應用研究所

考試科目（代碼）：計算機概論（2201）

　　*請在【答案卷、卡】作答

1. (5%)
   The following message was originally transmitted with odd parity in each short string of five bits. In which strings have errors definitely occurred?
   11001 11011 10110 00000 11111 10001 10101 00100 01110

2. (12%)
   Suppose the memory cells at addresses B0 to B8 in the 16-bit machine (described in Appendix A in page 6) contain the (hexadecimal) bit patterns given in the following table:

Address	Contents
B0	13
B1	B8
B2	A3
B3	02
B4	33
B5	B8
B6	C0
B7	00
B8	0F

   (1) (4%) If the program counter starts at B0, what bit pattern is in register 3 after the first instruction has been executed?
   (2) (8%) What bit pattern is in memory cell B8 when the halt instruction is executed?

3. (6%)
   Would greater throughput be achieved by a system running two processes in a multi-programming environment if both processes were I/O-bound or if one were I/O-bound and the other were compute-bound? Why?

4. (8%)
   (1) (4%) What is the similarity between deadlock and starvation?
   (2) (4%) What is the difference between deadlock and starvation?

5. (5%)
   In the blank next to each phrase, write the term from the following list that is best described by the phrase.

A. cloud;	B. router;	C. search engine;	D. internet;
E. UDP;	F. XML;	G. protocol;	H. ISP;
I. HTML;	J. Ethernet;		

   _____ (1) A network of networks
   _____ (2) A "format" for markup languages
   _____ (3) A means of connecting networks to form an internet
   _____ (4) A means of implementing a network with the bus topology
   _____ (5) A protocol for the transport layer

6. (6%)
   Answer the following questions regarding the TCP/IP hierarchy.
   (1) Which layer of the TCP/IP hierarchy actually transmits a message?
   A. Application B. Transport C. Network D. Link
   (2) Which layer of the TCP/IP hierarchy chops messages into units whose size is compatible with the Internet?
   A. Application B. Transport C. Network D. Link
   (3) Which layer of the TCP/IP hierarchy decides the direction in which message segments are transferred across the Internet?
   A. Application B. Transport C. Network D. Link

(4) Which layer of the TCP/IP hierarchy presents incoming messages to the computer user?
A. Application B. Transport C. Network D. Link

(5) Which layer of the TCP/IP hierarchy reassembles messages as their pieces arrive at the destination?
A. Application B. Transport C. Network D. Link

(6) Which layer of the TCP/IP hierarchy is responsible for obtaining the correct address for a message's destination?
A. Application B. Transport C. Network D. Link

7. (6%)

(1) (3%) Is the collection of statements (S OR ¬P), (Q → P), (Q OR ¬T), and (T OR S) consistent?

(2) (3%) Is the collection of statements (Q OR ¬S), (T OR S), ¬P, (P OR ¬T), and (P OR ¬Q) consistent?

8. (5%)
Suppose the points (1, 0, 0), (1, 1, 1), and (1, 0, 2) are the vertices of a planar patch. Which of the following line segments is/are normal to the surface of the patch?

(A) The line segment from (1, 1, 1) to (2, 1, 1)

(B) The line segment from (1, 0, 2) to (0, 0, 2)

(C) The line segment from (1, 0, 0) to (1, 1, 1)

(D) The line segment from (1, 0, 0) to (1, 1, 0)

(E) The line segment from (0, 0, 1) to (0, 1, 2)

9. (6%)
Consider a neuron that has three inputs and one output. The values of the inputs and the output are either 0 or 1. Adjust the weights and threshold value of the neuron so that its output is 1 if and only if at least two of its inputs are 1s.

10. (8%)
Suppose you have two buckets B1 and B2. B1 has a capacity of exactly three liters; B2 has a capacity of five liters. You can pour water from one bucket to another, empty a bucket, or fill a bucket at any time. Your problem is to place exactly four liters of water in the five-liter bucket B2. Describe how this problem could be framed as a production system with necessary states and rules. Show a small portion of the state graph (including at least five states) of this problem.

11. (12%)
The Josephus numbers are the numbers in the integer sequence 1, 1, 3, 1, 3, 5, 7, 1, 3, 5, 7, 9, 11, 13, 15, 1, …, in which each number J(n) is defined by the recurrence: J(1)=1, and J(2n)=2J(n)-1 and J(2n+1)=2J(n)+1 for n≥1.

(1) (6%) Please design an iterative algorithm to compute the Josephus number J(n).
(2) (6%) Please design a recursive algorithm to compute the Josephus number J(n).

12. (12%)
A stack is a list in which entries are inserted and removed only at the head. A queue is a list in which the entries are removed only at the head and new entries are inserted only at the tail. A singly linked list is an ordered set of data elements, each containing a link (or pointer) to its successor.

(1) (6%) Please design an algorithm to implement a stack using a singly linked list, where an entry is inserted in O(1) time and deleted in O(1) time.

(2) (6%) Please design an algorithm to implement a queue using a singly linked list, where an entry is inserted in O(1) time and deleted in O(1) time.

13. (9%)

(1) (3%) Please explain what a Turing machine is.

(2) (6%) Design a Turing machine that multiplies the value binarily represented on the tape by 2.

Appendix A

Op-code	Operand	Description
1	RXY	LOAD the register R with the bit pattern found in the memory cell whose address is XY. *Example:* 14A3 would cause the contents of the memory cell located at address A3 to be placed in register 4.
2	RXY	LOAD the register R with the bit pattern XY. *Example:* 20A3 would cause the value A3 to be placed in register 0.
3	RXY	STORE the bit pattern found in register R in the memory cell whose address is XY. *Example:* 35B1 would cause the contents of register 5 to be placed in the memory cell whose address is B1.
4	0RS	MOVE the bit pattern found in register R to register S. *Example:* 40A4 would cause the contents of register A to be copied into register 4.
5	RST	ADD the bit patterns in registers S and T as though they were two's complement representations and leave the result in register R. *Example:* 5726 would cause the binary values in registers 2 and 6 to be added and the sum placed in register 7.
6	RST	ADD the bit patterns in registers S and T as though they represented values in floating-point notation and leave the floating-point result in register R. *Example:* 634E would cause the values in registers 4 and E to be added as floating-point values and the result to be placed in register 3.
7	RST	OR the bit patterns in registers S and T and place the result in register R. *Example:* 7CB4 would cause the result of ORing the contents of registers B and 4 to be placed in register C.
8	RST	AND the bit patterns in register S and T and place the result in register R. *Example:* 8045 would cause the result of ANDing the contents of registers 4 and 5 to be placed in register 0.
9	RST	EXCLUSIVE OR the bit patterns in registers S and T and place the result in register R. *Example:* 95F3 would cause the result of EXCLUSIVE ORing the contents of registers F and 3 to be placed in register 5.
A	R0X	ROTATE the bit pattern in register R one bit to the right X times. Each time place the bit that started at the low-order end at the high-order end. *Example:* A403 would cause the contents of register 4 to be rotated 3 bits to the right in a circular fashion.
B	RXY	JUMP to the instruction located in the memory cell at address XY if the bit pattern in register R is equal to the bit pattern in register number 0. Otherwise, continue with the normal sequence of execution. (The jump is implemented by copying XY into the program counter during the execute phase.) *Example:* B43C would first compare the contents of register 4 with the contents of register 0. If the two were equal, the pattern 3C would be placed in the program counter so that the next instruction executed would be the one located at that memory address. Otherwise, nothing would be done and program execution would continue in its normal sequence.
C	000	HALT execution. *Example:* C000 would cause program execution to stop.