

國立清華大學命題紙

99 學年度 資訊工程學系 碩士班入學考試

科目 計算機系統 科目代碼 1902 共 5 頁，第 1 頁 \*請在【答案卷卡】作答

1. (CPU scheduling 8%) Assume context switching takes negligible time. Consider the following four processes, with the length of the CPU-burst time given in milliseconds:

Process	Arrival Time	Burst Time
P <sub>1</sub>	0	8
P <sub>2</sub>	1	4
P <sub>3</sub>	2	9
P <sub>4</sub>	3	5

- a. (4%) In this example, how long is the average waiting time a *non-preemptive* Shortest-Job-First (SJF) scheduling would result in? (The average waiting time is defined as the sum of the waiting times for the processes divided by the number of the processes.) Calculate the average waiting time.
- b. (4%) In this example, how long is the average waiting time a *preemptive* SJF scheduling (also known as Shortest-Remaining-Time-First scheduling) would result in? Calculate the average waiting time.
2. (5%) Paging and segmentation are both memory-management schemes. Several architectures implement segmentation and paging at the same time. However, it does not make sense to perform paging before segmentation. Explain the reason *briefly*.
3. (Deadlock 12%) Consider a system with seven processes, 1 through 7, and six non-shared resources, R through W. All of the resources are non-sharable and of one instance each. The allocated resource(s) cannot be released until the process is done. The state of which resources are currently owned and which ones are currently being requested is as follows:
- Process 1 holds R and wants S.
  - Process 2 holds nothing but wants T.
  - Process 3 holds nothing but wants S.
  - Process 4 holds U and wants S and T.
  - Process 5 holds T and wants V.
  - Process 6 holds W and wants S.
  - Process 7 holds V and wants U.

Please answer the following questions:

- a. (4%) What are the four necessary conditions for deadlock?
- b. (4%) Please draw the corresponding resource-allocation graph by copying the following graph to your answer sheet and *adding the corresponding arrows*

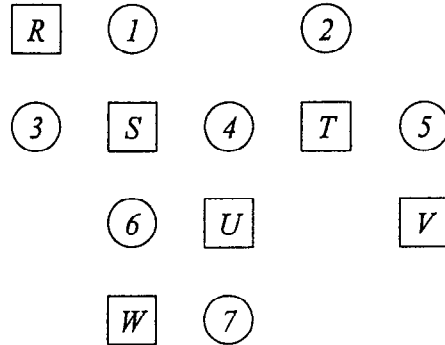
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(request edges and assignment edges).



- c. (4%) Does this system have deadlock? If so, list all the processes involved in the deadlock.
4. (10%) A computer has a virtual memory of  $2^{32}$  bytes. The computer also has  $2^{28}$  bytes of physical memory. The virtual memory is implemented by paging and the page size is 4096 bytes.
- a. (5%) What is the minimum size of the page table (in bits) on this computer if you want to guarantee that the virtual memory system works. (There is no score if you only give the size. You need to explain how the answer is found)
- b. (5%) Is it possible to design a good page replacement algorithm such that the average memory access time of the virtual memory system is better than the system that the virtual memory is removed (it means that the computer access the physical memory directly.). (There is no score if you only answer yes or no. You need to explain why you give such an answer)
5. (15%)
- a. (5%) What is the difference between a trap and a hardware interrupt?
- b. (5%) The process synchronization problem is a major research problem for modern Operating System. Assume that a computer does not have hardware interrupt, do you think the process synchronization problem no longer exists for such a computer? (There is no score if you only answer yes or no. You need to explain why you give such an answer)
- c. (5%) For a computer with no hardware interrupt, is it possible to implement a multi-tasking Operating System? Please note that the computer still provide trap and the performance of the Operating System is not considered. (No score for yes or no answer. If your answer is yes, you need to describe how to do it. If your answer is no, you need to explain why it is not possible.)
6. (4%) The following figure shows an implementation of ALU. Please give the 4-bit control value for the following operations. Fill out the blanks.

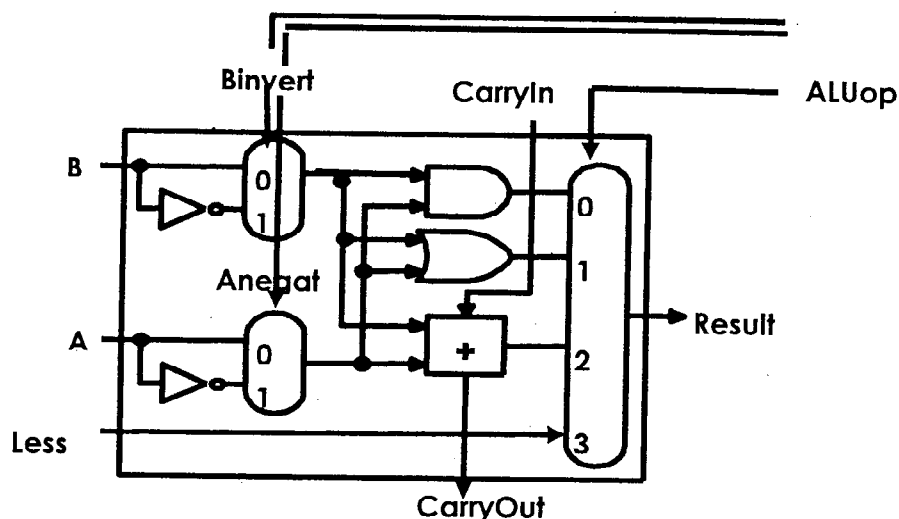
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Operations	4 bits (Anegat, Binvert, ALUOp)
$A \text{ sub } B$	
$A \text{ nand } B$	



7. (8%) Let  $a$ ,  $b$ ,  $c$  be three 8-bit operands to a carry save adder and their values be  $a = 00010110$ ,  $b = 01101101$  and  $c = 01001110$ .
  - a. (4%) What are the two outputs of this carry save adder?
  - b. (4%) Given the above carry save adder as basic building block, please show the block diagram of  $8 \times 8$  Wallace-tree multiplier with minimum delay.
8. (8%) Given a 5-stage pipelined data-path where register-read is performed at the second stage, ALU computation the third stage, memory read/write the fourth stage and register write the fifth stage. Consider the following MIPS instruction sequences:

lw	\$4, 100(\$4)	# \$4 $\leftarrow$ memory[\$4 + 100]
sw	\$4, 100(\$4)	# memory[\$4 + 100] $\leftarrow$ \$4
add	\$4, \$4, \$4	# \$4 $\leftarrow$ \$4 + \$4

  - a. (4%) Indicate the type of dependency that causes data hazard.
  - b. (4%) Assume there is no forwarding in the pipelined processor. Add *nop* instructions to the above codes so that the hazard is removed.
9. (4%) Control signals can be implemented by using Finite State Machine. However, for a five-stage pipelined data-path, the number of states is very large and it is not feasible to enumerate all states. Please describe how to implement the control of the above pipelined processor.

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10. (8%) Consider the design of a 500MHz multi-cycle microprocessor targeting the specific application such that the statistics of instructions is listed as follows:

	Cycles	Percentage in the Specific Application
Multiplication	12	25%
Arithmetic	3	20%
Load/Store	4	30%
Others	5	25%

- a. (4%) What percentage of time does the microprocessor spend doing multiplication?
  - b. (4%) The goal of your team is to improve the microprocessor. One of your team members indicate that the number of cycles required for multiplication can be reduced from 12 to 8, but it will require a 20% increase in the cycle time. What is the speedup with this modification?
11. (2%) Assume that a single cycle datapath with the critical path of 10ns can be partitioned into arbitrary number of balanced stages for pipelining, and there is no dependency between instructions. If the pipelining will introduce an additional 1ns delay to each stage. What is the speedup for the 4-stage pipelined datapath when compared with the single-cycle one?
12. (8%) Assume that the processor system consists of the microprocessor, cache, bus and main memory, running at 800MHz. A cache block has 32 words and one word has 4 bytes. Given the memory access parameters as follows:
- 1 memory bus clock cycle to send the address;
  - 20 memory bus clock cycles for each memory access initiated;
  - 1 memory bus clock cycle to send a word of data.

Consider three typical memory systems, i.e., (1) one-word-wide memory organization, (2) wide memory organization with main memory width of four words and (3) interleaved memory organization with four memory banks.

- a. (4%) Which memory organization has the smallest number of bytes transferred per bus clock cycle? And what is the number.
  - b. (4%) Suppose that the processor with a 32-word block size has an effective miss rate per instruction of 0.5%. Assume that the CPI without cache misses is 1.5. Which memory organization has the largest speedup when compared with the one-word-wide memory organization? And what is the speedup?
13. (8%) Costs of network topologies include the number of switches, the number of links on a switch to connect to the network, the data width per link, etc. Its performance includes the latency on an unloaded network to send/receive a message, the throughput, delays caused by contention, etc. Networks are normally drawn as graphs, with each arc representing a link. The processor-memory node is shown as a black square, and the switch is shown as a circle.
- a. (4%) For single-stage networks, one processor is placed at every switch node.

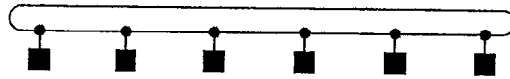
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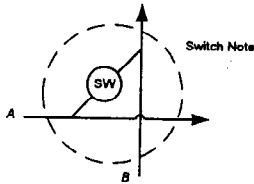
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For example, one of popular network topologies is ring (see the following figure). List and draw two other single-stage network topologies.



- b. (4%) On the other hand, multistage networks include Crossbar and Omega network, where processors and switches are separate. Assume the switch node controls whether the unidirectional links, A and B, connect to each other or not, as shown in the following figure.



Consider there are 8 processors, draw the Crossbar and Omega network topologies, list the number of switches required, and compare the advantage/disadvantage between the two topologies.