國　立　清　華　大　學　命　題　紙

97 學年度 資訊工程學 系（所）＿＿＿＿＿＿ 組碩士班入學考試

科目 計算機系統 科目代碼 2002 共 4 頁第 1 頁 *請在【答案卷卡】內作答

1. (5%) In what situations would use memory as a RAM disk be more useful than using it as a disk cache?

2. (10%) The following program segment can be used to provide mutual exclusion that satisfies the bounded-waiting requirement. Please write the missing instructions in **A** and **B**.

```
boolean waiting [n] = {FALSE};
boolean lock = FALSE;

do {
    waiting[i] = TRUE;
    key = TRUE;
    while (waiting[i] && key)
        Swap(&lock, &key);

    A;

    /* critical section */
    j = (i+1) % n;
    while ((j != i) && !waiting[j])
        j = (j+1) % n;

    if (j == i)
        lock = FALSE;
    else
        B;

  /* remainder section */
} while (TRUE);

Void Swap (boolean *a, boolean *b){
    boolean temp = *a;
    *a = *b;
    *b = temp;
 }
```

3. (5%) Explain why fairness is an important goal in a time-sharing system?

4. (8%) Consider a system consisting of resources of types A and B being shared by n processes P_1, P_2, ..., P_n. Resources can be requested and released by processes only one process at a time. A process P_i $(1 \le i \le n)$ may request at most $Max_{i,A}$ and $Max_{i,B}$ instances of resources of types A and B, respectively, where $Max_{i,A}$, $Max_{i,B} \ge 1$. However, a process P_i cannot be allocated any instance of resources of type B until it has been allocated $Max_{i,A}$ instances of resources of type A. What is the minimum number of instances of resources of types A and the minimum number of instances of resources of type B to guarantee that the system is deadlock free?

5. (8%) Let n processes P_1, P_2, ..., P_n with the length of the CPU burst time b_1, b_2, ..., b_n arrive at time a_1, a_2, ..., a_n, respectively. Suppose that $a_i < a_{i+1} < a_i+b_i$. What is the average waiting time (over all processes) for the first-come, first-served scheduling algorithm?

6. (12%) Let R be a reference string consisting of 6 different pages.
   (a) (2%) What is the minimum number of page faults for an optimal page-replacement strategy with 4 page frames if the length of R is 500?
   (b) (2%) What is the maximum number of page faults for an optimal page-replacement strategy with 4 page frames if the length of R is 500?
   (c) (8%) What is the maximum number of page faults (shown in a closed form) for an optimal page-replacement strategy with 4 page frames if the length of R is n?

7. (10%) The following questions are about computer arithmetic.
   (a) (5%) Perform $-2_{ten} \times 3_{ten}$ (both numbers are given in decimal) by first converting the numbers to the 4-bit two's complement ones and then using Booth's algorithm to get the 8-bit product.
   (b) (5%) Convert the IEEE 754 single precision floating-point number C0F40000, represented in hexadecimal, to its equivalent decimal number.

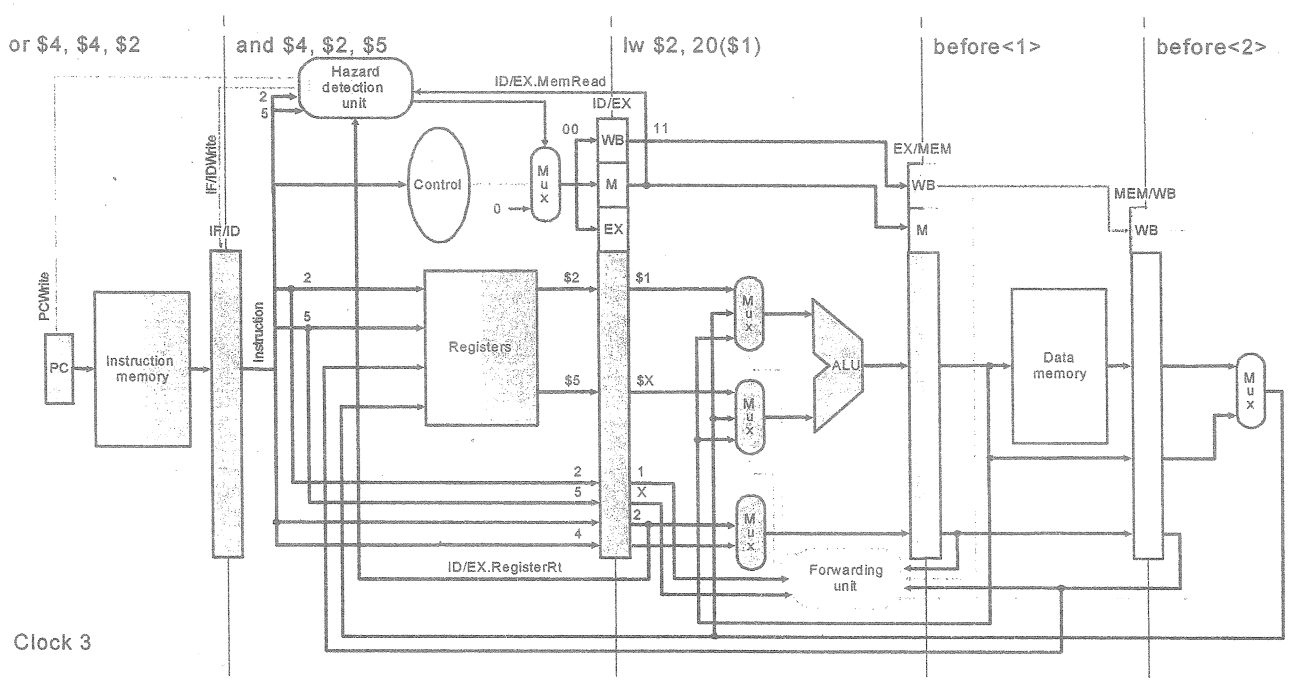
8. (6%) The following questions are about finite state machines.
   (a) (2%) A sequential circuit is to output 1 when the amount of 1's received at the input is an even number (≥ 0); otherwise the output is 0. What is the minimum number of states for the circuit?
   (b) (2%) Given a Moore machine with 3 states, how many different state assignments are there if 2 flip-flops are used to encode the states of the machine?
   (c) (2%) Given a Mealy machine with 5 input bits, 2 flip-flops, and 8 output bits, what is the maximum number of different patterns that can be observed on the machine's outputs?

9. (8%) Company ABC tests a computer product by repeatedly running a program that takes 80 seconds to execute. Of this execution time, 30% is used for memory access instructions, 40% for arithmetic instructions, and 30% for other tasks. Suppose the company is going to enhance the product, and there are two possible improvements: the first one is to make arithmetic instructions run 4 times faster than before, and the second one is to make memory access instructions run 3 times faster than before.
   (a) (4%) What will the speedup be if the improvement on memory access is made?
   (b) (4%) What will the speedup be if both improvement techniques are used?

10. (10%) Consider the following MIPS instruction sequence:

```
lw  $2, 20($1)        // $2 ← Memory[$1 + 20]
add $4, $2, $5        // $4 ← $2 + $5
```

The input operand to `add`, i.e. `$2`, depends on the output operand of `lw`. If this instruction sequence is executed in a 5-stage pipeline as shown below, the input operand `$2` to `add` will not be ready from `lw`. The execution will be incorrect. The design of the following circuit will *stall* the pipeline by inserting a "pipeline bubble" so that the output operand from `lw` can be forwarded to `add` in time.
   (a) (5%) Explain how the circuit works to insert a bubble between `lw` and `add` in the pipeline.
   (b) (5%) Suppose the circuit does not insert a bubble and let the instruction following the `lw` to continue executing, even if they are dependant. Explain how the compiler can do to ensure the correctness of the execution.



11. (a) (4%) Explain what a translation-lookaside buffer (TLB) does?
    (b) (4%) Use the diagram of problem 10 as a reference to draw another diagram to show where the TLB should appear in the pipeline.

12. (10%) Suppose the loop in the following program segment will be executed 3 times and exit to the label `Exit`. Each instruction is 32-bit long.

```
        and    $t1, $s3, $s3
        or     $t2, $t1, $s2
Loop:   add    $t3, $t2, $s6
        sub    $t0, $s2, $s6
        bne    $t0, $s5, Exit       // go to Exit if $t0 ≠ $s5
        add    $s3, $s3, $s4
        j      Loop
Exit:     …
```

Suppose the above code segment is initially stored in the memory. When it is executed, the instructions are loaded into the instruction cache. The instruction cache has 4 blocks in total; each block is 32-bit long. It is organized as a 2-way set associative cache.

(a) (6%) Trace the execution of this code segment and mark the instructions that will cause a cache miss. Note that the instructions inside the loop will be executed multiple times.

(b) (4%) For the above misses, identify which ones are compulsory misses and which ones are conflict misses.