國 立 清 華 大 學 命 題 紙

95 學年度 資訊工程學系（所） _____ 組碩士班入學考試

科目 計算機系統 科目代碼 2602 共 4 頁第 1 頁 *請在【答案卷卡】內作答

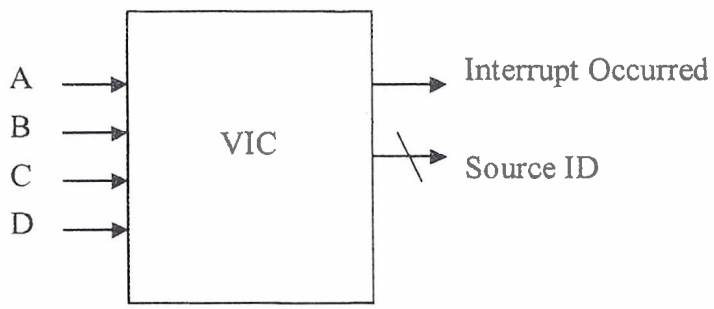
1. (7%) Design an array multiplier that multiplies two 3-bit integers in two's complement format and produces one 6-bit integer also in two's complement format.

2. (8%) Design a synchronous sequential machine that has one input X(t) and one output Y(t). Y(t) should be 1 if the machine has seen more 1s than 0s in the input over the past 3 time steps, and 0 otherwise. Below is a sample sequence:

t	0	1	2	3	4	5	6	7	8	9	10
X(t)	0	1	0	1	1	0	1	0	1	0	1
Y(t)	-	-	-	0	1	1	1	1	0	1	0

Hint: Use a 3-bit shift register.

3. (10%) Design a vector-interrupt controller (VIC) that has four interrupt sources, A, B, C and D with fixed priority A > B > C > D. In case of any interrupt occurred, the VIC should output the ID of the interrupting source with the highest priority. For example, if (A, B, C, D) = (0, 1, 0, 1), then the VIC should set "Interrupt Occurred" to 1 and "Source ID" to 01 indicating that B is the interrupt source for the host to serve. On the other hand, if (A, B, C, D) = (0, 0, 0, 0), then the VIC should set "Interrupt Occurred" to 0 indicating that no service is required.

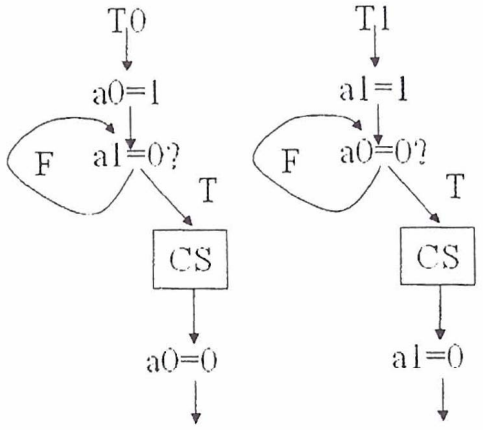


4. (12%) Consider a loop branch that branches nine times in a row, then is not taken once. Assume that we are using a dynamic branch prediction scheme.
   (a) (4%) What is prediction accuracy for this branch if a simple 1-bit prediction scheme is used?
   (b) (4%) What is prediction accuracy for this branch if a 2-bit prediction scheme is used?
   (c) (4%) Please draw the finite state machine for a 2-bit prediction scheme.

5. (5%) What feature of a write-through cache makes it more desirable than a write-back cache in a multiprocessor system (with a shared memory)? On the other hand, what feature of a write-back makes it more desirable than a write-through cache in the same system?

6. (8%) Consider a fully associative cache and a direct mapped cache with the same cache size.
   (a) (4%) Explain which one has a lower cache miss rate and why?
   (b) (4%) The majority of processor caches today are direct-mapped, two-way set associative, or four-way set associative, but not fully associative. Why?

7. (19%) The critical-section problem is to design a protocol that the processes can use to cooperate. Please answer the following questions.
   (a) (3%) What requirements a correct solution to the critical-section problem must satisfy?
   (b) (4%) Does the algorithm shown below satisfy the three requirements? If not, which requirements are violated? Why?



   (c) (4%) Which requirement may be violated if the wait and signal operations shown below are not executed atomically? Why?

```
typedef struct {
        int values;
        struct process *L;
}semaphore;

void wait (semaphore S) {
    S.value--;
    if (S.value<0) {
        add this process to S.L;
        block();
    }
}
```

```
void signal (semaphore S) {
    S.value++;
    if (S.value<=0) {
        remove a process P from S.L;
        wakeup(P);
    }
}
```

(d) (4%) Consider three concurrently running process: P1 with a statement S1, P2 with a statement S2, and P3 with a statement S3. Please use semaphores to solve the synchronization problem so that S1 is executed only after S3 has completed and S3 is executed only after S2 has completed.

(e) (4%) Two processes may be deadlocked if a semaphore is implemented with a waiting queue. Please show an example to illustrate this situation.

8. (6%) Consider a system consisting of *m* resources of the same type that are shared by *n* processes, each of which needs at most *k* resources. Please show the condition such that the system is guaranteed to be deadlock-free. Briefly explain why your condition can guarantee a deadlock-free system.

9. (10%) Consider the following C code:

```
main()
{    int   sum = 0, v;
     char *p;

     p = (char *) malloc(20);
     while (scanf("%s", p) == 1)
     {    v = atoi(p);
          v = power2(v);
          printf("\t %d \n", sum += v);
     }
     exit(0)
}
```

```
int power2(int x)
{
        return x * x;
}
```

(a) (4%) Identify the statements in the above code which will cause system calls in typical operating systems.

(b) (6%) Draw a flowchart to show the flow of operations starting from the user process, kernel IO subsystem, device driver, interrupt handler, until device controller and back, when the above scanf() function is called.

10. (6%) Consider using a computer without hardware support for virtual memory, e.g. TLB, LRU counters, etc. List the possible memory accesses, and for each access the associated operations, when the CPU issues a write to a virtual address. Assume that the corresponding page table and pages have already been loaded into the memory. Assume also that the virtual memory

uses write-back and LRU for page replacement.

11. (9%) A computer has the following parameters. The CPU has a clock rate of 1 GHz. The cache has a block size of W bytes and an average access time of X ns/byte. The virtual memory has a page size of Y KB, and the average disk transfer rate is Z KB/ms.
    (a) (6%) Give each of the four parameters a reasonable and representative numerical value, and then use the values to estimate the time to serve a page fault and that to serve a cache miss. (Please note the units of the parameters and make additional assumptions if necessary.)
    (b) (3%) Use the above estimations to explain why page faults will result in context switches while cache misses usually only stall the CPU.