

國立清華大學命題紙

九十三年學年度 資訊工程學 系(所) _____ 組碩士班入學考試

科目 計算機系統 科號 3002 共 5 頁第 1 頁 *請在試卷【答案卷】內作答

1. (15%) Consider a logical-address of 2048 pages of 1024 words (4 bytes) each, mapped onto a physical memory of 64 frames. Please answer the following questions assuming that the smallest memory allocation unit is one byte (8 bits).
 - (a) (5%) How many bits are in the logical address and in the physical address?
 - (b) (5%) Assuming that a one-level page table is used, how many bytes are required by the page table?
 - (c) (5%) Assuming a 2-level page table is used and the first-level table has 32 entries, what is the minimal amount of memory (in bytes) required by the page tables?

2. (5%) Please explain the difference between a general-purpose operating system (such as Linux or NT), an embedded operating system (such as ucLinux or Nucleus), and a microkernel operating system (such as Mach).

3. (5%)
 - (a) (3%) A correct solution to the critical section problem must satisfy three requirements. List each of them.
 - (b) (2%) The following code is not a correct solution to a 2-process critical section problem. Explain which requirement is not satisfied.

```
do {  
    flag[i] = TRUE;  
    while (flag[j]);  
        critical section  
    flag[i] = FALSE;  
    remainder section  
} while (1);
```

4. (10%) Three processes, P1, P2, and P3, arrive at the times indicated in the following:
P1: arrival time 0.4ms, burst time 4.0ms
P2: arrival time 0.2ms, burst time 6.0ms
P3: arrival time 1.0ms, burst time 1.0ms
 - (a) (5%) Calculate the average turnaround time in millisecond using the non-preemptive FCFS scheduling;
 - (b) (5%) Calculate the average turnaround time in millisecond using the non-preemptive SJF scheduling.

NOTE: Turnaround time is defined as finishing time minus arrival time.

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科目 計算機系統 科號 3002 共 5 頁第 2 頁 *請在試卷【答案卷】內作答

5. (6%) There are three popular methods to allocate disk blocks for a file: contiguous, linked, and indexed. Please use three drawings to depict them, respectively. In each drawing, please explain the method and list its pros and cons.
6. (9%) In a virtual memory system using a demand-paged method, the page table is stored in registers. It is found that 50% of the pages to be replaced are modified, i.e. dirty. If there is no page fault, the memory access time is 10 nanoseconds. To service a page fault, the OS may encounter the following three situations with the required elapsed time:
- (1) An empty page is available requiring 50 microseconds;
 - (2) The replaced page is not dirty requiring 50 microseconds;
 - (3) The replaced page is dirty requiring 500 microseconds.
- (a) (6%) Assuming the page fault rate is 0.00002, or 0.002%. What is the effective access time in nanoseconds
- (b) (3%) If a user process P is running without any interrupt or timeout, please identify all of those statements that are always true:
- (I) The OS does not issue a page fault when the page being referenced by P is in the cache memory.
 - (II) The OS does not issue a page fault when the page being referenced by P is in the physical memory.
 - (III) The OS does not issue a page fault when the page being referenced by P is in the main memory.
 - (IV) The OS does not issue a page fault when the page being referenced by P is in the logical memory.
 - (V) The OS does not issue a page fault when the page being referenced by P is in the hard disk storage.

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科目 計算機系統 科號 302 共 5 頁第 3 頁 *請在試卷【答案卷】內作答

7. (10%) Consider a 16-bit processor which includes a register file of 4 registers (**R0-R3**). **R3** is hardwired to act as the program counter. This processor has only one instruction "**Rd = Rs + #immed**", and is implemented using a 3-stage pipeline.

- (1) Instruction Fetch (IF): Instruction Register (**IR**) = **MEM[R3]**; **R3+=2**;
- (2) Instruction Decoding (ID): Decode **IR** to determine **Rd**, **Rs**, and **#immed**.
- (3) Execution (EX): Execute **Rd = Rs + #immed**.

The operation **R3+=2** of the IF-stage and the write-back of **Rd** in the EX-stage occur at the very end of each clock cycle (CC). If there is a conflict (both **EX:Rd** and **IF:R3** are writing to the register **R3**), the write-back of **R3** overrides the operation **R3+=2** in the IF-stage. Consider executing the following instruction sequence and its timing chart of the pipeline operation

Instruction Address	Instruction	Clock Cycle (CC)						
		1	2	3	4	5	6	7
0x0100	R0 = R3 + #0x001	IF	ID	EX				
0x0102	R3 = R3 + #0x010		IF	ID	EX			
0x0104	R2 = R3 + #0x100			IF	ID	EX		
0x0106	R2 = R0 + #0x200				IF	ID	EX	
0x????	R1 = R0 + #0x300					IF	ID	EX

- (a). (2%) Right after **CC=1**, what is the hexadecimal value stored in the register **R3**?
- (b). (2%) Right after **CC=3**, what is the hexadecimal value stored in the register **R0**?
- (c). (2%) Right after **CC=4**, what is the hexadecimal value stored in the register **R3**?
- (d). (2%) Right after **CC=6**, what is the hexadecimal value stored in the register **R2**?
- (e). (2%) What is the hexadecimal address of last instruction in the table?

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科目 計算機系統 科號 3002 共 5 頁第 4 頁 *請在試卷【答案卷】內作答

8. (5%) Suppose you are given an instruction set architecture (ISA) which includes only two instruction formats

SUB Rd, Rs, #immed /* Rd = Rs - #immed */

ADD Rd, Rs, Rt /* Rd = Rs + Rt */

where **Rd** is the 8-bit destination register, **Rs** and **Rt** are the 8-bit source registers, and the immediate value can be an integer between -4 to 3. How would you translate each of the following pseudo-instructions into one or multiple real ISA instructions?

- (a) (1%) **MOV** **Rd, Rs** /* Rd = Rs */
- (b) (1%) **INC** **Rd** /* Rd++ */
- (c) (1%) **MOV** **Rd, Rs lsl 1** /* Rd = Rs << 1; i.e., left shift*/
- (d) (2%) **CLEAR** **Rd** /* Rd = 0 */
9. (5%) Suppose Booth's algorithm is used as our approach to multiplying two 8-bit unsigned integer numbers. How many additions and subtractions are needed to multiply 123 by 123?
10. (5%) In a computer memory hierarchy, determine which of the following five combinations of events (for locating a page of memory) in the cache, TLB, page table, and main memory are possible to occur. Answer Yes or No to each of (a), (b), (c), (d) and (e). (1% each)

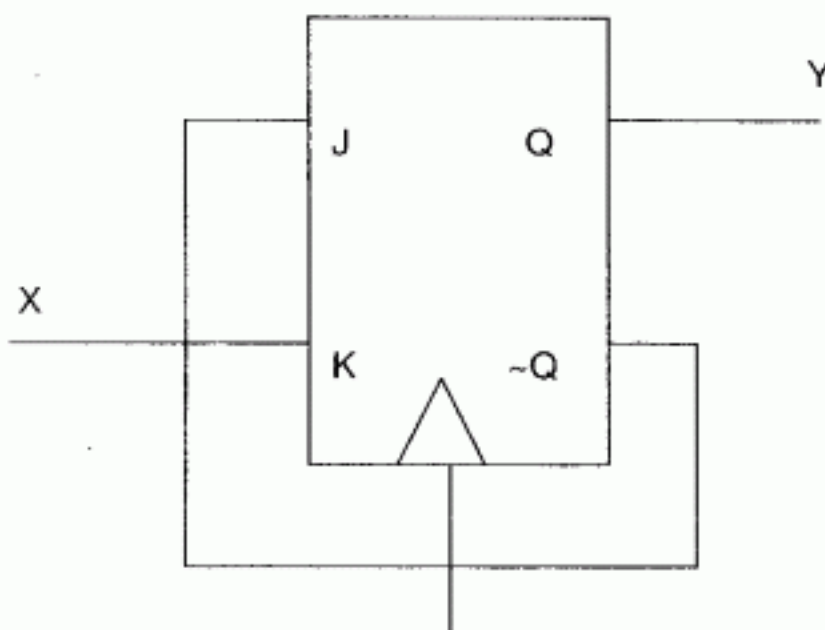
	TLB	Page Table	Cache	Main Memory
(a).	Hit	Hit	Hit	Miss
(b).	Hit	Hit	Miss	Miss
(c).	Miss	Hit	Hit	Miss
(d).	Miss	Miss	Hit	Hit
(e).	Hit	Miss	Hit	Hit

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11. (10%) For a CPU to effectively handle service requests from peripheral devices, vectored interrupt is a popular mechanism. To implement vectored interrupt function, a combinational circuit called priority encoder is commonly used.
- (a) (4%) What is the operation principle of vectored interrupt?
- (b) (6%) What is a priority encoder? How is it different from an ordinary encoder?
12. (10%) Analyze the following synchronous sequential circuit. Assume the positive-edge-triggered JK flip-flop output is initially 0. **What is the output sequence at Y** when the input sequence at X is 0111 0001?



13. (5%) **Design a state transition diagram** for a Mealy-style finite state machine with one input X and one output Y that recognizes the occurrence of the pattern 10^*1 , where 0^* denotes one or more consecutive 0. For example, both 10001 and 101 match the pattern while 11 does not, and, if the machine sees 1100 1011 1011 at X, then it should produce 0000 1010 0010 at Y.

NOTE: Just draw the state transition diagram and clearly specify your initial state.