國 立 清 華 大 學 命 題 紙

九十一學年度 資訊工程學 系（所） 組碩士班研究生招生考試

科目 計算機系統 科號 2702 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. (10%)
   (a) (5%) What is *asynchronous I/O*?
   (b) (5%) If asynchronous I/O is performed on a high-speed I/O device, the CPU will need 2 microseconds (for example) to respond to each interrupt, with interrupts arriving from the I/O device at every 4 microseconds (for example). That would not leave much time for process execution. How do modern computer systems solve this problem?

2. (5%) What is the *dispatch latency* of an operating system?

3. (10%)
   (a) (5%) In an acyclic-graph directory structure, several directories may *share* a common sub-directory. If a sub-directory is asked to be deleted, we only remove a correspondent link without deleting it, unless it is not a shared one. What is the simplest way to determine whether a sub-directory is shared or not when it is asked to be deleted?
   (b) (5%) Does your answer in (a) work for a general graph directory structure? Please explain briefly.

4. (5%) We call a grammar an *ambiguous grammar* if there are more than one parse tree for a given string of tokens. The following grammar is an ambiguous grammar. Please rewrite it to an unambiguous one.
   <S> → d | <F>
   <F> → a <S> b <S>
   <F> → a <S>

5. (10%) The heap memory has been commonly used for dynamic memory allocation in modern operating systems. Please
   (a) (3%) explain the usage of heap
   (b) (3%) describe the definition of heap fragmentation and its cause
   (c) (4%) propose a solution for heap fragmentation.

6. (10%) Consider the following page-reference string:

   1, 3, 2, 5, 6, 7, 2, 4, 5, 2, 5, 3, 1, 2

   How many page faults would occur with each of the three page replacement algorithms if there are 4 frames in the system? Here we assume that all frames are initially empty.

   (a) (3%) LRU replacement

   (b) (3%) FIFO replacement

   (c) (4%) Optimal replacement

7. (6%) In general, which type of processors, RISC or CISC, has a simpler control unit? Please explain briefly.

8. (6%) Briefly explain the main differences between DSP processors and general-purpose processors (e.g., Pentium).

9. (6%) Which type of design scheme, edge-triggered or level-sensitive, is more suitable for high-speed logic designs? Please explain briefly.

10. (7%) Briefly explain why variable instructions often complicate the pipelining design?

11. (5%) Explain how a branch instruction changes the flow of control, by describing what registers it checks or changes.

12. (5%) Sort the following elements of the memory hierarchy in order of increasing access time. (In other words, start from the fastest.) (a) L1 Cache (b) L2 Cache (c) Network (d) Main Memory (e) CPU Registers (f) Hard Disk

13. (5%) A non-pipelined CPU can finish an instruction in 8 ns (nanosecond). It may be changed to a 5-stage pipelined version where each stage takes 2 ns to finish. In the pipelined version, an individual instruction takes 10 ns to finish (i.e. 2 ns * 5 stages). But a program will run faster in the pipelined version than in the non-pipelined version. Explain why.

14. (5%) Which of the following cannot be EXACTLY represented by a single-precision floating-point number? Please explain briefly. (You may assume that floating-point numbers have 23-bit significands and 8-bit exponents.)
(a) 0 (b) 102 (c) 102.5 (d) 10.2 (e) 10.25

15. (5%) Assuming that you are designing a low-end video display card. Your design calls for data transfer rate of 133Mbyte/second. You need to make a decision between using the PCI bus and using the AGP port. The specification of PCI bus is 133Mbyte/second. The AGP port is capable of 533Mbyte/second. The design using the AGP port will incur a slightly higher cost than the design using the PCI bus. Will you use the PCI bus or the AGP port? Please explain briefly.