1. Let the address bus and data bus of a CPU be 32 bits. A 32-bit address is used to access one byte of memory.

   a) (10%) Draw a figure to show the organization of a two-way set associative cache which has eight-word blocks and a total size of 16 K bytes, where one word consists of 4 bytes and a block is the minimum unit of information that can be either present or not present in the cache.

   b) (5%) Draw a figure to explain how different portions of a memory address are used to access a word in the cache.

2. a) (3%) What is a synchronous I/O bus?

   b) (3%) What is an asynchronous I/O bus?

   c) (4%) Compare the advantages and disadvantages of synchronous and asynchronous I/O buses.

3. (7%)

Suppose we have a microprocessor with a 5-stage instruction pipeline: IF (instruction fetch), ID (instruction decode and operand fetch), EXE (ALU execute), MEM (memory access), and WB (result register write back). When this processor executes the following sequenece of instructions:

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sub  R2,R1,R3     // R2 ← R1 - R3
and  R12,R2,R5    // R12 ← R2 and R5
or   R13,R6,R2    // R13 ← R6 or R2
add  R14,R2,R2    // R14 ← R2 + R2
add  R15,R3,R2    // R15 ← R3 + R2
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the last four instructions are all dependent on the result (R2) of the first instruction.

(a) Suppose we allow these instructions enter the pipeline without any special mechanism to resolve their dependences. Which instructions will fetch a wrong operand from the not-yet-ready register R2?

(b) Suppose we resolve the dependences by "stalling" the dependent instructions until the needed operand is written back to the register file. Then for how many cycles does it take for the processor to execute these five instructions? (Count the cycles starting when the first instruction enters the pipeline until the last exits.)

4. (10%)

Many processors designed based on the RISC concept have very regular instruction formats. For example, a 32-bit MIPS architecture has three instruction formats, all are 32 bits long and have a 6-bit opcode. The R-format and I-format have respectively two and three 5-bit register fields in fixed positions.

(a) Many computer designers argue that such an instruction set architecture makes CPU design simple and can improve performance faster. Please give three reasons to support their arguments.

(b) Despite the above arguments, in reality we find that x86 processors (a CISC architecture) still perform very well and improve performance very fast. Why?

5. (8%)

The time for a processor to execute a program is given by the following formula:

execution time = instruction count * CPI * clock cycle time

where CPI is cycle per instruction. Now suppose a processor supports three classes of instructions: A, B, and C. Their CPI are 1, 2, and 3, respectively. Suppose further that there are two different computers both using the processor as their CPU. When two benchmark programs are executed on these two computers, we obtain the following data:

Instructions executed (in millions)

	Program 1			Program 2		
Machne	A	B	C	A	B	C
1	5	1	1	10	2	2
2	10	1	1	5	3	3

Assume that both computers run a 100-MHz clock. Summarize the performance of each of these two computers using an arithmetic mean. Which machine runs faster?

6. (5%) Explain the functionalities for Monitor and Semaphore. Also what are their differences?

7. (10%) Write pseudo codes to demonstrate how to emulate a Monitor by using Semaphores.

8. (5%) Suppose that the head of a moving-head disk with 200 tracks, numbered 0 to 199, is currently serving a request at track 143 and has just finished a request at track 125. The queue of requests is kept in the FIFO order:

   86, 147, 91, 177, 94, 150, 102, 175, 130.

   Explain which of the following algorithms will have the minimum amount of head movements to satisfy the above requests.

   (a) FCFS

   (b) SCAN

   (c) LOOK

   (d) C-SCAN.

9. (5%) Explain the key issues in supporting a real-time operating system for embedded systems.

10.(9%)

Explain the mapping of virtual addresses to real addresses under paging by

(a) direct mapping

(b) associative mapping

(c) combined direct/associated mapping

11. - 18. (2% each) Point out the three most related terms

11. (a) mutual exclusion (b) capability (c) critical section (d) rendezvous (e) protection.

12. (a) preemption (b) virtual memory (c) working set (d) fragmentation (e) round-robin scheduling.

13. (a) X.25 (b) SSTF (c) CSMA/CD (d) C-SCAN (e) TCP/IP

14. (a) authentication (b) segmentation (c) authorization (d) cryptography (e) cache.

15. (a) response time (b) utilization (c) arrival rate (d) deadlock (e) starvation.

16. (a) circular wait (b) deadlock (c) object-oriented (d) portability (e) reusability.

17 (a) process (b) blocked state (c) prefetch (d) ready state (e) processor

18. (a) data dictionary (b) dirty bit (c) join operation (d) query language (e) locality.