八十五學年度 資訊科學 系（所） 組碩士班研究生入學考試

科目 計算機系統 科號 0803 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. (11%) Answer the following short questions. **Explain your answers; otherwise you will not get any point.**

   (a) (2%) Which of the following three representations for the value of 28.0_{10} has the greatest precision? (i) $0.0034_8 \times 8^4$ (ii) $0.0340_8 \times 8^3$ (iii) $0.3400_8 \times 8^2$.

   (b) (2%) In a 64-bit byte-addressable machine, how much does the program count (PC) need to be incremented after the current instruction is fetched?

   (c) (2%) How many instruction bits are required to specify two operand registers and one result register in a machine that has 32 general-purpose registers?

   (d) (3%) A *displacement* addressing mode has an offset specified relative to a base value. An example is shown below:

   ```
   Add R4,100(R1)          (meaning:  R4 <- R4+M[100+R1])
   ```

   The value 100 in the above example is called the *displacement*. In a machine in which all instructions are 32 bits with a 6-bit opcode, what is the maximum value of the displacement. Assume that the machine has 32 general-purpose registers.

   (e) (2%) When an instruction actually contains the effective address of an operand, the address is an *absolute address*. How can the displacement addressing be used to do absolute addressing? Use the above example to explain your idea.

2. (6%) Consider the design of dynamic random-access memory (DRAM).

   (a) (2%) Explain why DRAM needs refreshing.

   (b) (4%) A certain DRAM chip organizes its memory cells into a 128×8 2D array. It requires refreshing at least once every 2 ms. Refreshing is accomplished by internally reading and writing all 128 rows of memory cells in sequence. Suppose the memory cycle time is 500 ns. What is the overhead of refreshing? (i.e., what percentage of time does the chip do refreshing?)

3. (4%) Suppose we want to write an image file of 1MB to hard disk. The software overhead of initiating the transfer takes 0.1 ms. The disk rotates in 10 ms, has 50 10KB sectors per track and 10 tracks per cylinder. Cylinder seek time is 15 ms, but the disk can switch from one track to another of the same cylinder in essentially zero time. Suppose the image file will be written to contiguous sectors of the disk. Determine the amount of time to write this image file to the disk.

4. (4%) A pipelined processor can fetch one instruction for execution in each cycle. Due to its internal organization, the pipeline will always fetch and execute the instruction immediately following a conditional branch. To avoid executing wrong instructions, a simple-minded solution is to always insert an NOP (no-operation) after the conditional branch, e.g.,:

   ```
         ADD  R1,R2,R3        ;R1 <-- R2+R3
         BGTZ R1,Loop         ;branch to Loop if R1>0
         NOP                  ;always executed
         SUB  R4,R5,R6
   Loop: ...
   ```

   Try to rearrange the above instructions so as to eliminate NOP. Explain under what conditions you can make this rearrangement.

5. What will be the decimal numbers for 0001 and 0000 ?

   (a) (1%) sign magnitude

   (b) (2%) ones complement

   (c) (2%) twos complement.

6. Assume that $X = x_0x_1x_2$ and $Y = y_0y_1y_2$ are unsigned integers. Design a 3-bit combinational multiplier for $P = XY$ with AND gates and full adders.

   (a) (1%) How many bits are required for the product P ?

   (b) (1%) How Many AND gates are required ?

   (c) (1%) How many full adders are required ?

   (d) (5%) Draw the logic circuit with full adders and AND gates.

   (e) (2%) Assume that the delay of AND gate is d' and the delay of a full adder is d. What is the multiplication time ?

7. There are CDROMs, RAMs(random access memory), hard disks and caches in a computer system.

   (a) (2%) Which one is the main memory ?

   (b) (2%) Which one is the immediate temporary storage between the processor registers and main memory ?

   (c) (2%) Which are secondary memory ?

   (d) (2%) Which one can be virtual memory ?

   (e) (2%) Which one should have the fast access time ?

8. (a) Why do we need dynamic linking? (5%)

   (b) How do a compiler and the operating system cooperate to support dynamic linking? (5%)

   (c) Does any PC-based operating system support dynamic linking? If so, how? (5%)

9. (a) Define different kinds of elapse time for accessing direct access devices such as hard disks. (3%)

   (b) What kind of elapse time is the most critical? (2%)

   (c) Describe a simple scheduling policy for minimizing such elapse time. (5%)

八十五學年度 資訊科學 系（所） 組碩士班研究生入學考試

科目 計算機系統 科號 0803 共 3 頁第 3 頁 *請在試卷【答案卷】內作答

10.(10%) Does the following algorithm satisfy all the three requirements for the critical-section problem ? Why ?

Assume that the *n* processes share the following variables:

var *flag*:**array**[0..1] of (*idle* ,*want-in, in-cs)*

turn: 0..n-1;

All the elements of *flag* are initially *idle*; the initial value of *turn* is immaterial (between 0 and *n-1*). The following program is for process *Pi*.:

```
var j: 0..n;
repeat
    repeat
        flag[i] := want-in;
        j:=turn;
        while j <> i
            do if flag[j] <> idle
                    then j := turn;
                    else j   := j+1 mod n;
        flag[i] := in-cs;
        j :=0;
        while (j < n) and (j = i or flag[j] <> in-cs) do j := j+1;
    until (j >= n) and (turn = i or flag[turn] =idle);
    turn := i;
        critical section
    j := turn+1 mod n;
    while (flag[j]≠idle) do j := j+1 mod n;
    turn := j;
    flag[i] := idle;
        remainder section
until false;
```

11.(4%) Should the long-term scheduler select a good process mix of I/O-bound and CPU- bound processes ? Why ?

12.(5%) Explain how the CSMA/CD protocol works. How the CSMA/CD protocol handles the frames collision problem ?

13.(6%) What (if any) relation holds between the following pairs of sets of scheduling algorithms ? For example, the FCFS algorithm is the RR algorithm with an infinite time quantum.

(a) Priority and SJF, (b) Priority and FCFS, (c) RR and SJF