國立清華大學 104 學年度碩士班入學考試試題

系所班組別：資訊工程學系

考試科目（代碼）：計算機系統（2002）

1. (6%) What resources in a computer are used when a thread is created? How do they differ from those used when a process is created?
2. (10%) Consider a variant of the round-robin (RR) CPU scheduling algorithm where the entries in the ready queues are pointers to the process control blocks (PCBs).
   (a) (3%) What would be the effect of putting multiple pointers to the same process in the ready queue?
   (b) (4%) What are the advantages and disadvantages of the scheme in (a)?
   (c) (3%) How can the basic RR CPU scheduling algorithm be modified to achieve the same effect of the scheme in (a)?
3. (8%) Suppose that a semaphore, *mutex*, which is initialized to 1, is used to solve the critical section problem. Consider the following three situations:
   (S1) a process omits the signal(*mutex*);
   (S2) a process omits the wait(*mutex*); and
   (S3) a process omits both the signal(*mutex*) and wait(*mutex*).
   (a) If (S1), or (S2), or (S3) is true, either (I) _____ is violated or (II) a _____ will occur. (Fill in each blank with one or two words in English.)
   (b) In which situations, (S1), (S2), or (S3), will (I) happen?
   (c) In which situations, (S1), (S2), or (S3), will (II) happen?
4. (4%) Name a common memory management technique (in English), other than compaction, that can be used to solve the problem of external fragmentation.
5. (5%) Consider a demand-paging memory management system that uses the additional-reference-bits algorithm for page replacement. Let b be the 8-bit byte that we keep for a page P. Let (t_1, t_2, t_3, ...) be the sequence of times at which b is updated. Suppose that the *decimal* value of b after the update at time t_{20} is 147. Assume that the numbers of references to the page P at the time intervals (t_{20}, t_{21}), (t_{21}, t_{22}), (t_{22}, t_{23}), (t_{23}, t_{24}), (t_{24}, t_{25}), (t_{25}, t_{26}), (t_{26}, t_{27}), (t_{27}, t_{28}) are, respectively, 0, 1, 2, 0, 3, 0, 4, 2. What is the *decimal* value of b after the update at t_{23}? Detailed explanation is necessary.
6. (4%) Describe how UNIX uses inode structure to allocate disk spaces, and why it can be beneficial for small files and large files.

7. (4%) Explain how RAID (Redundant Array of Independent Disks) can improve the reliability and performance of secondary storage systems.
8. (9%) There are many approaches to improve the performance of I/O, for example, using Direct Memory Access (DMA). Describe how DMA works to accelerate the I/O operations, and list three other approaches to improve the I/O performance.
9. (10%) In computers, floating-point numbers are expressed as the signed bit, exponent and fraction field. The bits of the fraction present a number between 0 and 1. Assume that the floating point numbers are 32 bits, with a bias of 127. Let x= 0.3125 and y = -0.09375 (in decimal).
   (a) (4%) Show the floating-point number presentation of x and y using hexadecimal representation.
   (b) (6%) Show the floating-point number presentation of $x*y$ using hexadecimal representation.
10. (6%) Two n-bit inputs *A[i]* and *B[i]* are combined by the two's-complement subtraction *(A-B)* with the subtraction result denoted as *Sub[i]*. The most significant bit *n-1* is the signed bit. *Bor(n-2)* denote the borrow from bit *n-2* to bit *n-3*. Indicate whether each of the following conditions is a valid test for two's complement overflow. (The condition must be true if and only if there is overflow.) Answer True or False for the following cases.
    (a) $A(n-1)$ *XOR* $B(n-1) = 1$ and $Sub(n-1) = 1$
    (b) $A(n-1)$ XOR $B(n-1) = Bor(n-2)$
    (c) $A(n-1)$ *XOR* $B(n-1) = 1$ and $Sub(n-1) \neq A(n-1)$
11. (6%) Assume a processor has a base CPI of 1.4, running at a clock rate of 4GHz. The access time of the main memory is 50ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. What will be the speedup after adding a secondary cache with a 5ns access time for either a hit or a miss? Assume that the miss rate to main memory can be reduced to 0.2%.
12. (4%) Consider a system with the virtual memory address of 32 bits, and the physical address of 28 bits. The page size is 2KB. Each page table entry is 4 bytes in size.
    (a) How many bits are in the page offset portion of the virtual address?
    (b) What is the total page table size?

13. (9%) A specific memory organization has the following memory access times:
    i. 1 memory bus clock cycle to send the address;
    ii. 10 memory bus clock cycle for each DRAM access initiated;
    iii. 1 memory bus clock cycle to send a word of data.

Assume that a cache block has eight words. Each word has four bytes.

(a) (5%) Increase the width of the memory organization (as well as the bus) can increase the memory bandwidth. Determine the smallest width of the memory organization in terms of bytes, such that the bandwidth (number of bytes transferred per bus clock cycles) for a single miss exceeds 1.2 bytes/cycle.

(b) (4%) Instead of increasing the width of memory, the interleaved memory organization can be used utilizing the advantage of multiple banks, each with one word wide. What is the bandwidth speedup of the interleaving scheme as compared with the original one-word-wide memory?

14. (15%) The `beq` instruction of MIPS will cause the processor to branch to execute from a target address if the contents of the two specified registers are equal:

```
beq $rs, $rt, Target        # branch to Target if $rs == $rt
```

It uses the I-type format shown below, where *Opcode* is 6-bit wide, *rs* and *rt* are 5-bit wide, and *Immediate* has 16 bits with the leftmost bit as the sign bit.

Opcode	*rs*	*rt*	*Immediate*

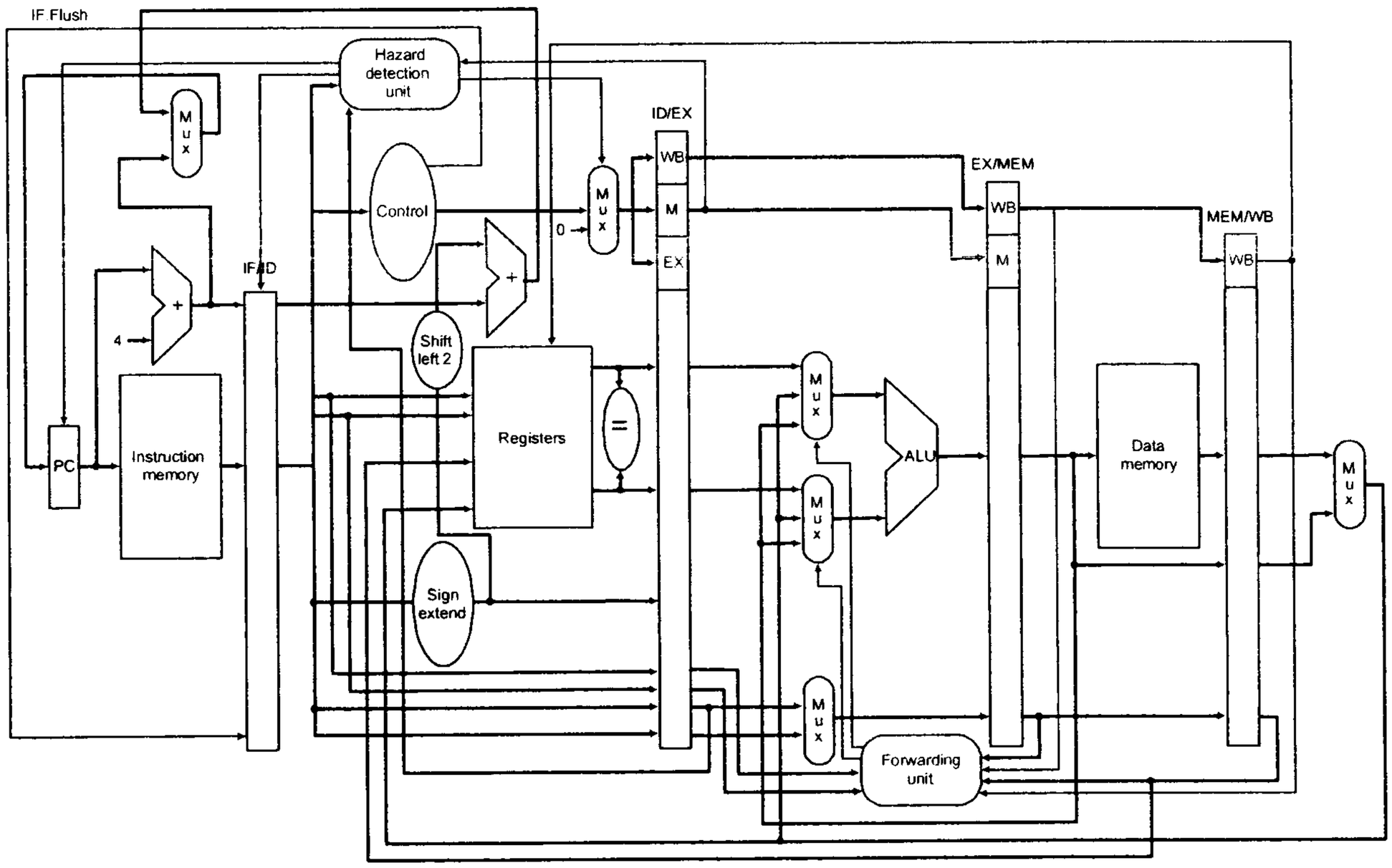
The target address of `beq` is calculated as *PC + (Immediate*4)*. Consider the pipelined implementation of the MIPS processor shown in the next page and answer the following questions.

(a) (3%) Explain the purpose of the Adder in the ID stage.

(b) (3%) Explain the purpose of the Mux in the IF stage.

(c) (4%) Explain the purpose of the IF.Flush control signal.

(d) (5%) Suppose we have a *branch target buffer*, which uses PC as the input, can always predict correctly whether a branch will take, and supply the target address. Draw a diagram to explain how the IF stage may be modified. (Hint: Consider the outputs of the branch target buffer and what existing components may be removed.)


IF.Flush
Hazard detection unit
M u x
Control
ID/EX
WB
M
EX
EX/MEM
MEM/WB
0
+
4
IF/ID
Shift left 2
PC
Instruction memory
Registers
=
ALU
Data memory
Sign extend
Forwarding unit