

國立清華大學 103 學年度碩士班入學考試試題

系所班組別：資訊工程學系碩士班(0521)

考試科目（代碼）：計算機系統(2102)

共 5 頁，第 1 頁 *請在【答案卷、卡】作答

1. (5%) A process can be in one of the following states: new, ready, waiting, running and terminated and the state transition events include admitted, interrupt, I/O completion, I/O wait, dispatch and exit. Please draw a diagram showing the life cycle of a process using above states and events.
2. (10%) Consider the following set of processes, with the length of the CPU-burst time given in milliseconds: The processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0. Please answer the following questions, given 2 scheduling algorithms, Shortest-Job-First (SJF) and Non-Preemptive Priority (a smaller priority number implies a higher priority):

Process	Burst Time	Priority
P1	10	3
P2	2	1
P3	4	3
P4	2	4
P5	6	2

- (a) (5%) Draw *Gantt charts* illustrating the execution of these processes using the two scheduling algorithms.
 - (b) (5%) What is the *turnaround* time of each process for each of the two scheduling algorithms?
3. (5%) Show that, if the wait() and signal() semaphore operations are not executed atomically, then mutual exclusion may be violated.

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共 5 頁，第 2 頁 *請在【答案卷、卡】作答

4. (5%) Two processes, A and B , each need three records, 1, 2, and 3, in a database. If A asks for them in the order 1, 2, 3, and B asks for them in the same order, deadlock is not possible. However, if B asks for them in the order 3, 2, 1, then the deadlock is possible. With three resources, there are $3!$ (=6) possible combinations each process can request the resources. What fraction of all combinations is guaranteed to be deadlock free?
5. (6%) What is the purpose of paging the page tables?
6. (4%) Consider a demand-paging system with the following time-measured utilizations: CPU utilization 25%, Paging disk 97%, Other I/O devices 10%. Which (if any) of the following will (probably) improve CPU utilization? Explain your answer.
 - (a) (2%) Install a faster CPU.
 - (b) (2%) Increase the degree of multiprogramming.
7. (10%) In an i-node based file system implementation, the i-node typically stores 12 direct block pointers, one 1-indirect (single-indirect) block pointer, one 2-indirect (double-indirect) block pointer, and one 3-indirect (triple-indirect) block pointer. Recall that an indirect block is a disk block storing an array of disk block addresses (i.e. pointers). The pointers in a 1-indirect block point to disk blocks that store file data. The pointers in a 2-indirect (or 3-indirect) block point to other 1-indirect (or 2-indirect) blocks. Suppose the file system is configured to use a block size of 2^{10} bytes and each pointer takes up 4-byte.
 - (a) (5%) What is the maximum number of pointers stored in a 1-indirect block?
 - (b) (5%) What is the maximum file size (in Bytes) that can be supported in the file system? Explain your calculation.

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共 5 頁，第 3 頁 *請在【答案卷、卡】作答

8. (5%) Consider a computer with a processor that operates at 4GHz (4×10^9 cycles/second). When a network packet arrives, the network card interrupts the CPU, which then processes the packet. The cost of the following sum to 10,000 cycles: a context switch to the interrupt handler, handling a packet, and the context switch out of the interrupt handler. A lot of other computers want to talk to this computer, and for a time, it receives 1,000 packets per second. Assume one interrupt per packet. What is the total percentage of the processor's cycles that are spent in interrupt-related code (meaning the context switching and packet handling)? Explain your answer briefly (for example, by showing your work).
9. (6%) A computer has 3 instruction classes. They are A, B and C. The A instruction class is 1 CPI (clock cycles per instruction), the B instruction is 2 CPI and the C instruction is 3 CPI. A program code has 5 millions of the A instruction class, 2 millions of the B instruction class and 3 millions of the C instruction class. Assume that the clock rate of the computer is 100 MHz. What is the execution time of the program code?
10. (2%) What is the decimal value of the 4-bit two's complement binary number 1010?
11. (a) (4%) A full adder has two 1-bit numbers x_i, y_i , a carry-in bit c_i , a sum bit z_i and a carry-out bit c_{i+1} . Write the equations of the sum bit z_i in terms of x_i, y_i , and c_i .
- (b) (4%) A 4-bit carry-look-ahead adder has two 4-bit binary numbers $x_3x_2x_1x_0$ and $y_3y_2y_1y_0$, a carry-in bit c_0 , the sum bits $z_3z_2z_1z_0$ and a carry-out bit c_4 . It can be formed from 4 stages, each of which is a full adder by replacing its output carry line c_i by two carry generate signals g_i and p_i , where $0 \leq i \leq 3$. Write the equation for the carry-out bit c_4 of the 4-bit carry-look-ahead adder in terms of c_0, g_i and p_i , where $0 \leq i \leq 3$.

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共 5 頁，第 4 頁 *請在【答案卷、卡】作答

12. (11%) In a data cache, consider what the cache must do on a write miss.
- (a) (4%) Describe two options for a write-through cache in response to a write miss.
 - (b) (4%) Describe a scenario that can benefit from each option listed in Part (a) above and briefly explain why.
 - (c) (3%) Describe the typical option for write-back cache in response to a write miss. Why are there fewer options than write-through caches?
13. (6%) If there is no mechanism for cache invalidation or for marking certain memory locations non-cacheable, the data cache and the DMA controller may not work properly together.
- (a) (3%) If the cache is a write-back cache, can something go wrong if the DMA controller performs a read? What about a write?
 - (b) (3%) If the cache is a write-through cache, can something go wrong if the DMA controller performs a read? How about a write?
14. (8%) Given a basic five-stage pipelined MIPS CPU with comparator with the branch address computing done at the ID stage and the following sequence of instructions. We assume that branch predictor always predicts next instruction and for the execution of #40 *beq* the prediction is not taken.

36: lw \$1, 8(\$4)	72: lw \$4, 50(\$7)
40: beq \$1, \$3, 7	76: add \$3, \$4, \$3
44: and \$12, \$2, \$5	80: or \$3, \$2, \$6
...	84: slt \$3, \$6, \$3

Please answer the following questions for execution from instruction #36 to #84.

- (a) (4%) Assume there is no forwarding in this pipelined processor. How many NOPs are inserted?
- (b) (4%) Assume full forwarding. How many NOPs are inserted?

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15. (4%) True or False

- (a) Like SMP, message-passing computers rely on locks for synchronization.
- (b) Both multithreading and multicore rely on parallelism to get more efficiency from a chip.
- (c) GPUs rely on graphics DRAM chips to reduce memory latency and thereby increase performance on graphics applications.
- (d) Shared memory multiprocessors cannot take advantage of job-level parallelism.

16. (5%) What are the values (0 or 1) of control signals generated by the control in the following graph?

instruction	AluSrc	RegWrite	MemRead	MemWrite	Branch
beq Rs, Rt, L					

