國　立　清　華　大　學　命　題　紙

97 學年度 通訊工程研究 系（所） 乙 組碩士班入學考試

科目 計算機系統 科目代碼 1903 共 2 頁第 1 頁 *請在【答案卷卡】內作答

1. (10%) A Gray code is a sequence of binary numbers with the property that no more than one bit changes in going from one element of the sequence to another. For example, here is a 3-bit binary Gray code: 000, 001, 011, 010, 110, 111, 101 and 100. Using three D-flip-flops and a PLA, construct a 3-bit Gray code counter that has two inputs: *reset*, which sets the counters to 000, and *inc*, which makes the counter go to the next value in the sequence. Note that the code is cyclic, so that the value after 100 in the sequence is 000.

2. (6%) (a)Average memory access time (AMAT) is the average time to access memory considering both hits and misses and the frequency of different accesses. It is defined as:

   AMAT = Time for a hit + Miss rate × Miss penalty

   If the machine A with a 10-ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time including hit detection of 1 clock cycle. Assume the read and write miss penalties are the same and ignore other write stalls. If the machine B has the miss rate 0.03 misses per reference by doubling the cache size. This causes the cache access time to increase to 1.2 clock cycles. Using the AMAT as a metric to determine which machine is better.
   (6%) (b) If the machine's clock cycle time must be changed to match that of a cache, which machine is better based on the measurement of execution time. Assume the machines are identical except for the clock rate and number of cache miss cycles; assume 1.5 references per instruction and a CPI without cache misses of 2. The miss penalty is 20 cycles for both machines.

3. (11%) Suppose we have a memory system that uses a 50-MHz clock. The memory transmits 8-word requests at the rate of 1 word per cycle. For reads from memory, the accesses occur as follows:
   1. 1 cycle to accept the address,
   2. 3cycles of latency, and
   3. 8 clock cycles to transmit the 8 words.

   For writes to memory, the accesses occur as follows:
   1. 1 cycle to accept the address,
   2. 2 cycles of latency,
   3. 8 clock cycles to transmit the 8 words, and
   4. 3 cycles to recover and write the error correction code.

   Find the maximum bandwidth in megabytes per second for an access pattern consisting of
   a. All reads from memory.
   b. All writes to memory.
   c. A mix of 65% reads from memory and 35% writes to memory.

4. (10%) Given a set of processes with known processing times. Suppose that all processes arrive at a computer at the same time. These processes are to be processed by the computer. Prove that the shortest-job-first scheduling algorithm gives the minimal average waiting time.

5. (5%) What is Belady's anomaly in a demand-paging system?

6. (8%) Explain the reason why the least recent used (LRU) page-replacement algorithm does not suffer from Belady's anomaly.

7. (10%) There are two methods for handling I/O devices, namely, polling and interrupt.
   (a) Under what situation is it more suitable to use polling?
   (b) Under what situation is it more suitable to use interrupt?

8. (12%) Hosts A and B are directly connected with a 200 Mbps link. Assume that there is no communication error on this link. There is one TCP connection between the two hosts, and Host A is sending to Host B an enormous file over this connection. Host A can send application data into the link at 100 Mbps but Host B can read out of its TCP receive buffer at a maximum rate of 50 Mbps. Describe the effect of TCP flow control for this network.

9. (10%) Consider a broadcast channel with N nodes and a transmission rate of R bps. Suppose the broadcast channel uses polling (with an additional polling node) for multiple access. Suppose the amount of time from when a node completes transmission until the subsequent node is permitted to transmit (that is, the polling delay) is d_{poll}. Suppose that within a polling round, a given node is allowed to transmit at most Q bits. What is the maximum throughput of the broadcast channel?

10. (12%) consider a 100 Mbps 100BASE-T Ethernet with all nodes directly connected to a hub. To have an efficiency of 0.50, what should be the maximum distance between a node and the hub? Assume that a frame length of 64 bytes and that there are no repeaters. Assume that the velocity of propagation in the medium is 1.8×10^8 m/sec. Does this maximum distance also ensure that a transmitting node A will be able to detect whether an other node transmitted while A was transmitting? Why and why not?