1. In the differential amplifier circuit as shown, all transistors are matched with parameters β=100, V_A=100 V, $V_{BE(on)}$=0.7 V, $V_{CE,sat}$=0.3 V.
   (1) Calculate the following parameters: (10%)
      a. g_m value of Q_1 and Q_2
      b. differential voltage gain $V_o/(V_1-V_2)$
      c. differential input resistance
   (2) Find the minimum input common mode voltage $V_{CM,min}$ and the output voltage swing $V_{o,min}$, and $V_{o,max}$. (9%)

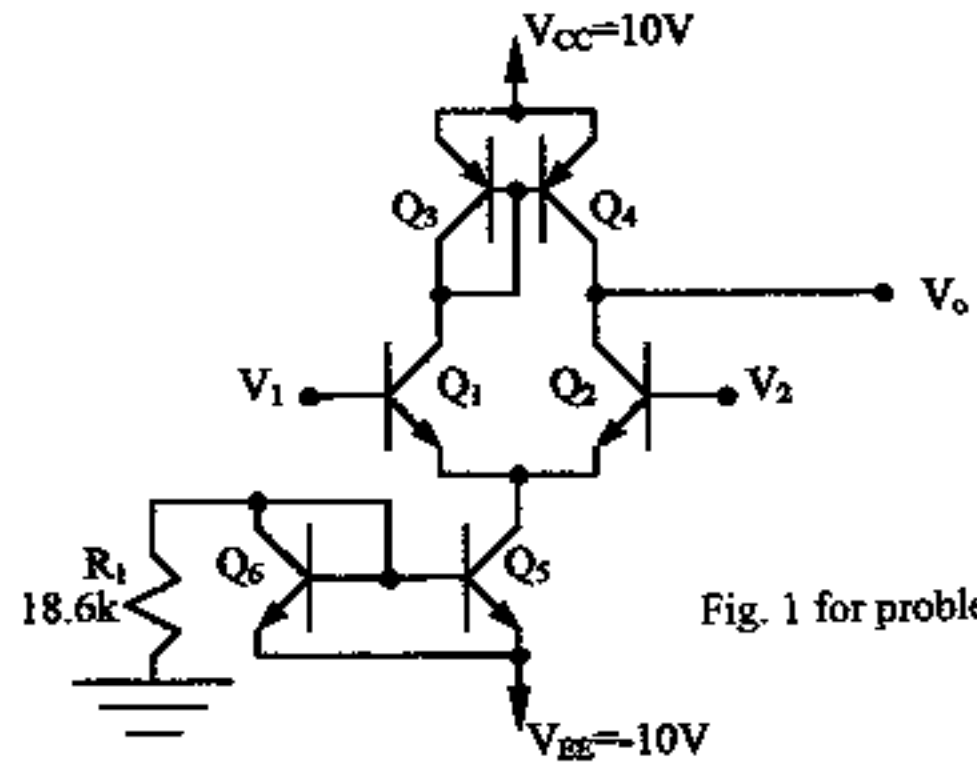

Fig. 1 for problem 1.

2. A common emitter amplifier was found to have a single-time-constant high frequency response with mid-band voltage gain of 40 dB and upper 3-dB frequency of 100 KHZ.
   (1) Sketch the Bode plot for the voltage gain |A| (3%)
   (2) Find $|A|_{dB}$ for frequencies at 400 KHZ and 4 MHz. (5%)

3. In the circuit, the op-amp is ideal and the BJT has $\beta=\infty$.
   (1) What is the feedback topology? Explain your reason.
   (2) Find the voltage gain V_o/V_s.
   (3) Find the power dissipation on the BJT when V_s=2 V.
   (8%)

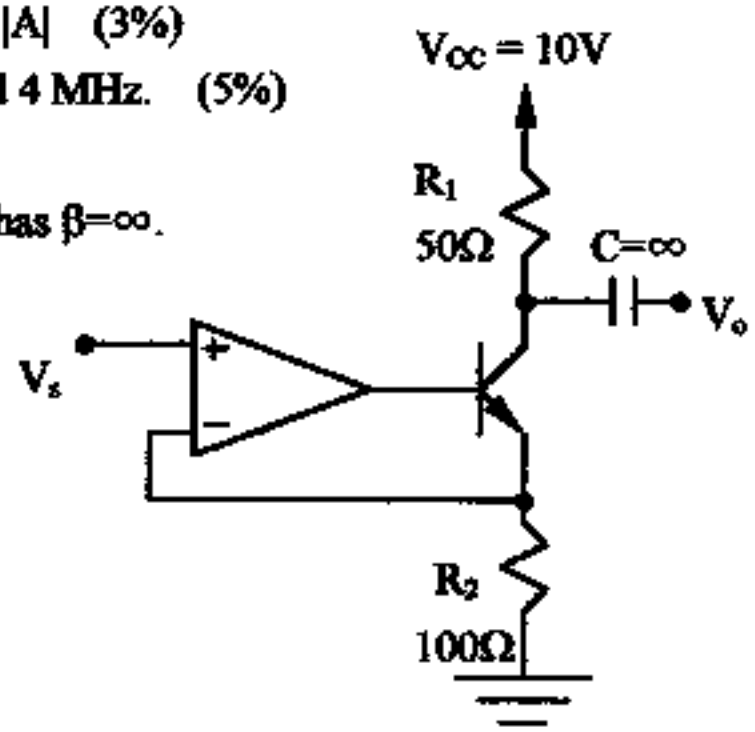

Fig. 2 for problem 3.

4. A lightly doped pn diode is used for light detector with $N_a=2\times10^{14}cm^{-3}$ and $N_d=1\times10^{16}$ cm^{-3}. Assume the depletion region widths in the p region and the n region are W_p and W_n, respectively.

(a) What is W_p/W_n?(5%)

(b) Find the maximum W_p and W_n that can be obtained if the junction breaks down at reverse bias voltage of 30V and assume the critical field for junction breakdown is 1×10^6 V/cm. (5%)

5. For a common-source stage with a resistor load is shown in Fig. 3 below. Assume $k_p=100\mu A/V^2$, W=20μm, L=1μm, $V_T=1V$ and neglect channel length modulation effect for M1.

(a) Find the input bias range within which M1 is in saturation.(5%)

(b) What is the maximum small-signal voltage gain of this circuit? (5%)

(c) Propose changes in the circuit parameters so the input bias range can be increased.(5%)

(d) Replace M1 with a BJT , Q1 with $Is=1\times10^{-15}A$ (neglect base current). Estimate the input bias range within which Q1 is in forward-active region. (5%) (FYI: ln2=0.69, ln3=1.1, ln5=1.6, ln7=1.9,ln10=2.3)

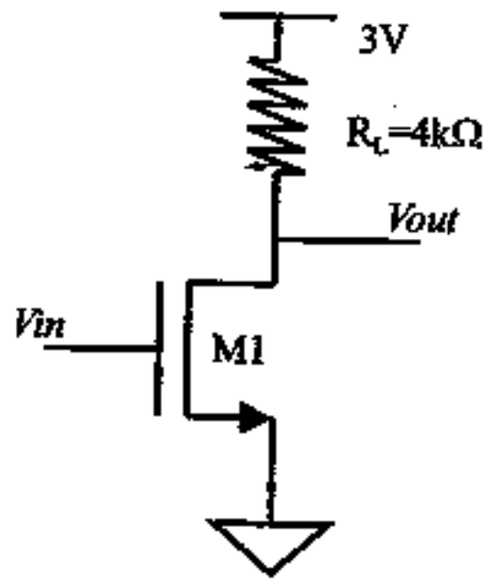

Fig.3 for problem 5.

6. For Fig. 4 below,

(a) Draw the Input-output plot with explanations. 5%

(b) What is this circuit's name? 5%

(c) What are the limitations/constraints of this circuit? 5%

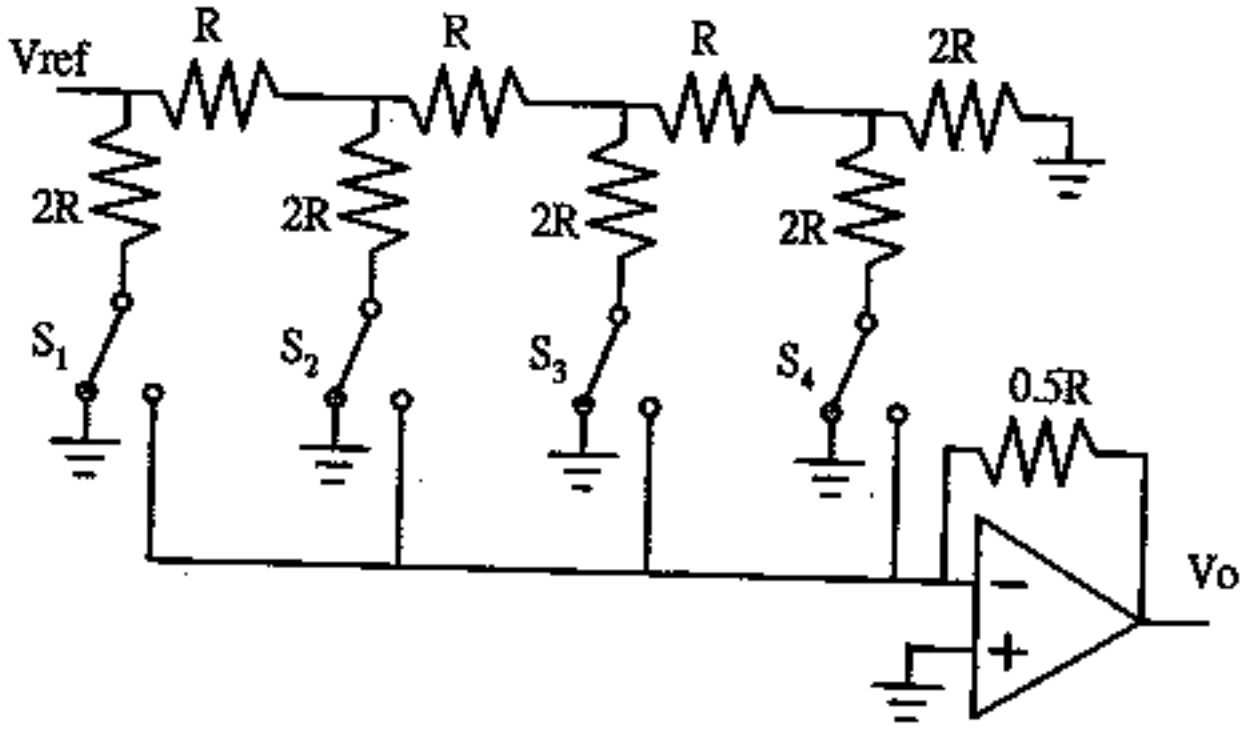

Fig. 4 for problem 6.

7. In Fig. 5, the saturated outputs for the ideal Op Amp are +10V and −10V,

(a) If Vref =0V, draw the Vi-Vo plot with explanations. (5%)

(b) If Vref =5V, draw the Vi-Vo plot with explanations. (5%)

(c) How do you get precise output level by using a resistor and two Zener diodes? 5%

(d)Also draw the Vi-Vo plot in (c) and show the values of the output levels with

$V_{Z,reverse}$ =5V and $V_{Z,\ forward}$=0.5V (5%)

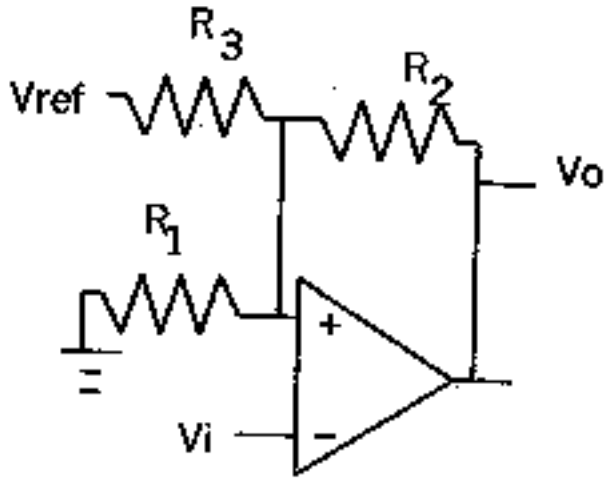

Fig. 5 for problem 7