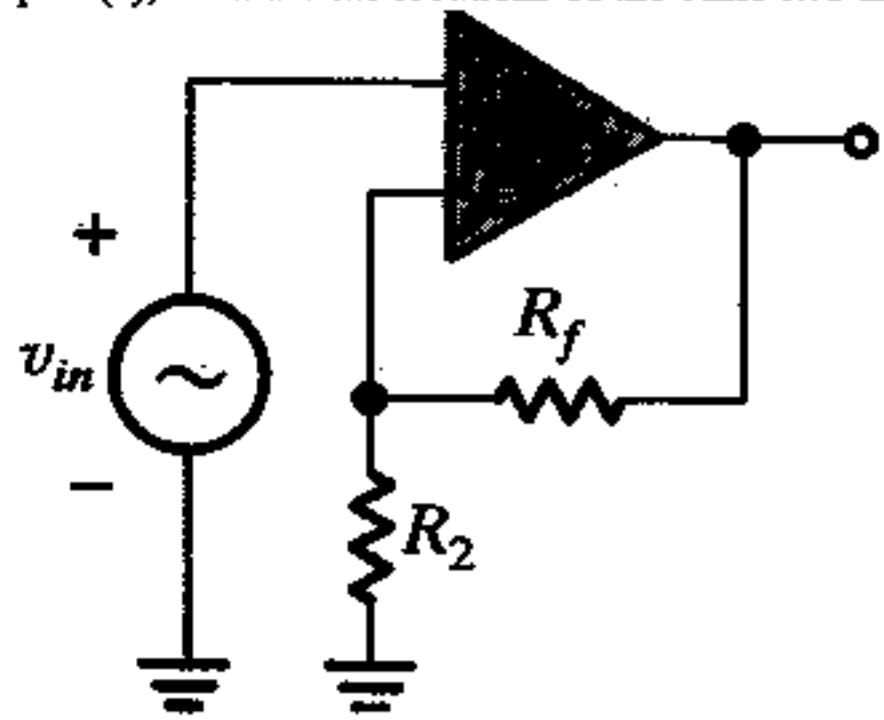
1. A MOS differential amplifier utilized a bias current I=25μA. The devices have V_t=1V, W=120 μm, L=6 μm and $\mu_n C_{ox}$ for this technology is 20 μA/V². Find V_{GS}, g_m, and the differential input voltage v_{id} for full current switching. (15%)

2. A non-inverting amplifier is constructed with R_2= 100 Ω and R_f adjustable. The op amp open-loop gain is $A_{OL}=10\alpha^3/[(s+\alpha)(s+2\alpha)^2]$

   (a) Find the value of R_f that will just place one of the closed-loop amplifier poles at s= −3α. (5%)

   (b) For the value of R_f chosen in part (a), what are the locations of the other two amplifier poles? (10%)

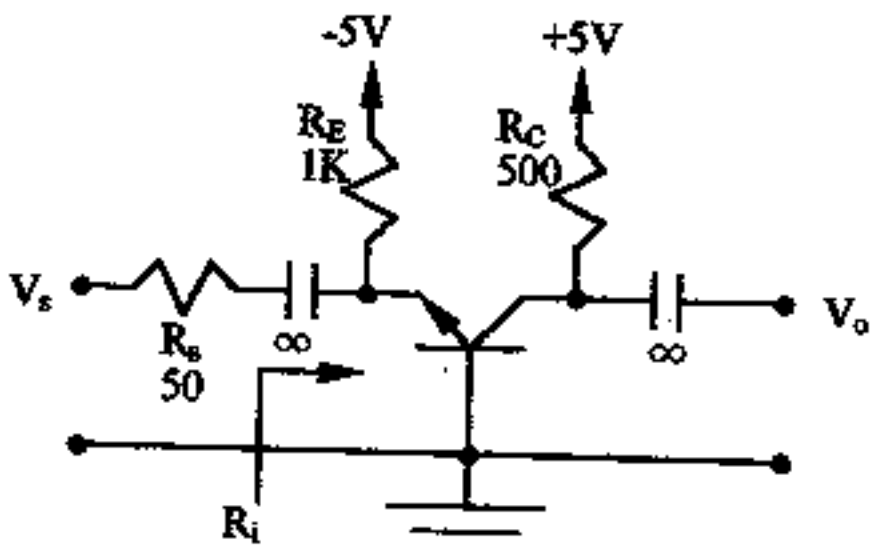


3. (25%) A BJT with β=100 is used in the circuit below with the voltage V_{BE}= 0.7V.

   (a) Determine the voltage V_{CB} and the transconductance g_m of the BJT. (8%)

   (b) Sketch the small signal equivalent circuit. (7%)

   (c) Find the voltage gain V_o/V_s and the input resistance R_i. (10%)



4.(10%)As shown in the Fig. 3, calculate Vo by neglect Rsc (Assuming that op amp 741 is ideal).

5.(20%)As shown in the Fig. 3, a voltage regulator is used to provide constant voltage Vo with maximum output current Io=0.5 A. The V_{BE} turn-on voltage for Q2 and Q3 are, respectively, 0.6V and 0.7V (at 25°C), respectively, with the $\partial V_{BE3(on)}/\partial T$=–2.5mV/°C

(a) Calculate the minimum load. (5%)

(b) At what temperature (°C) this voltage regulator will be thermal shut down?(5%)

(c) Mark the protection elements(5%)

(d) Calculate Rsc by neglect voltage over R2. (5%)

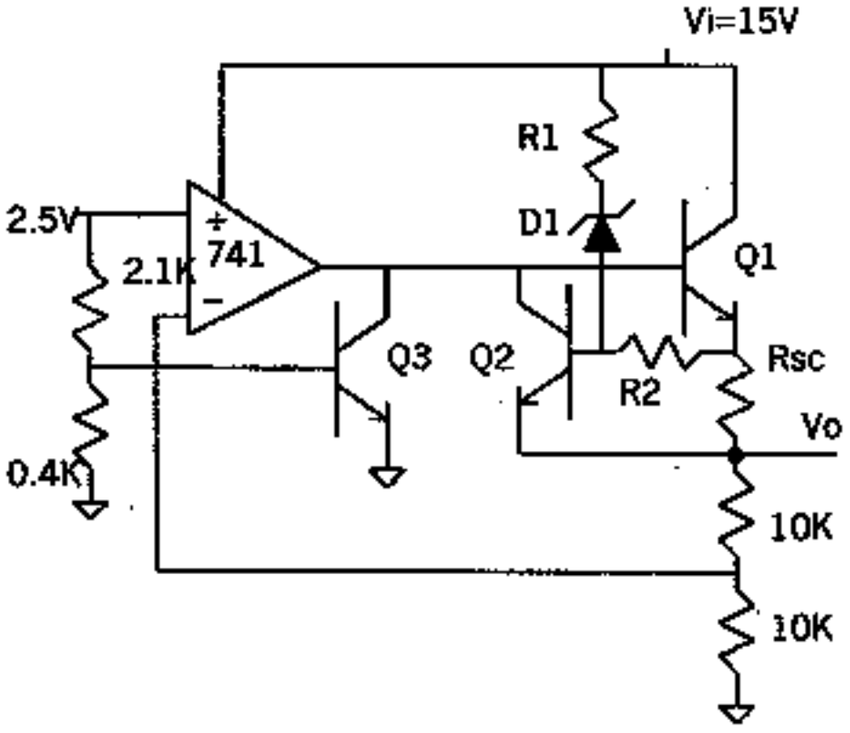


Fig. 3

6. (a) Draw the structure of a CMOS transmission gate in transistor level with each transistor as 4-node device(5%)

(b) Explain the operations if the values of the control signal are VDD and Ground. (10%)