國　立　清　華　大　學　命　題　紙

九十二學年度 工程與系統科學 系（所） 丁 組碩士班研究生招生考試

科目 電子學 科號 3903 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

（請注意!! 答題務必按題號順序）

1. (a) A Zener diode is generally used as a shunt regulator. For good regulation performance, should the conducting Zener resistance r_Z be high or low ? Why ? (b) If the input resistance R_{in} is low and the output resistance R_o is high for a voltage amplifier, a buffer stage will be generally introduced. How about the R_{in} and R_o for this buffer stage ? (Ans. in: high or low) Why ? (20%)
2. (a)Sketch the cell structures for SRAM and DRAM, respectively. Briefly compare the differences in chip density and refresh. (b)Sketch the cross section figure of EPROM. Where is the charge stored for the 0/1 data ? (20%)
3. Analyze the high-frequency response of the CMOS amplifier with I_{REF}= 0.1 mA as shown in Fig.3. For Q1, $\mu_n C_{ox}$= 90 μA/V^2, V_A= 12.8 V, W/L=100/1.6, Cgs= 0.2 pF, Cgd= 0.015 pF, and Cdb= 20 fF. For Q2, Cgd= 0.015 pF, Cdb= 36 fF, and $|V_A|$= 19.2 V. A stray capacitance of 0.3 pF exists between Vo and ground. Assume that the resistance of the input signal generator is negligibly small and the signal voltage at the gate of Q2 is zero. Find the frequency of the pole and zero.(20%)

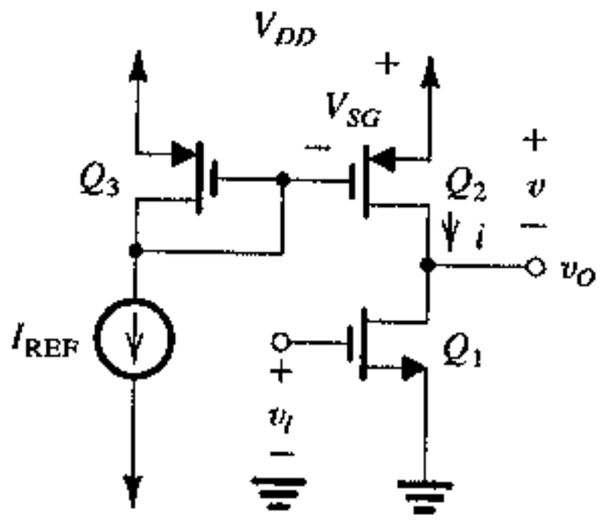

Fig. 3

4. A CMOS linear amplifier as in Fig.3 has the i-v and transfer characteristics shown in Fig.4. (a)Find the operation mode of Q_1 and Q_2, respectively. (Ans. in: off or triode or saturation), (b) For $V_{OA}= V_{DD}-(V_{SG} + V_t)$, does the threshold voltage V_t belong to Q_1 or Q_2 or Q_3 ? (c) For $V_{OB}= V_{IB}- V_t$, does the V_t belong to Q_1 or Q_2 or Q_3 ? (20%)

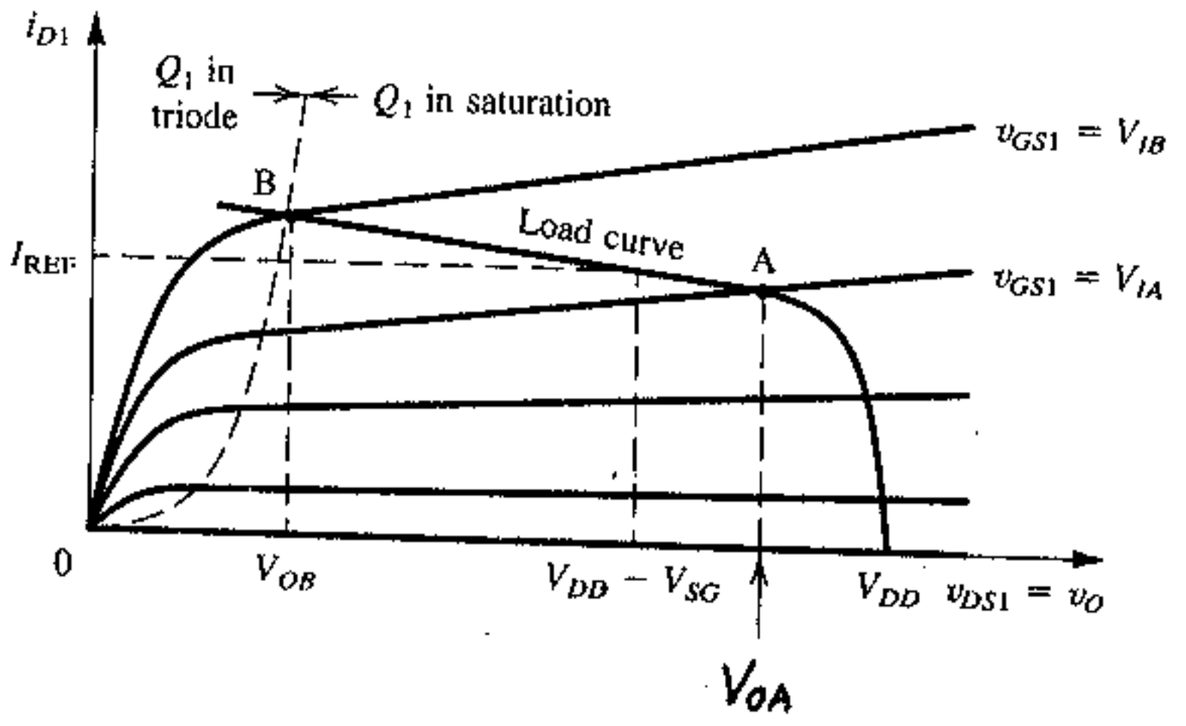

Fig. 4

5. In Fig.5 of ECL logic circuit with $V_{BE(on)}$=0.75V and β >=100 for all Q, find the V_R, V_{OL} (ie, V(0)). Why does a ECL logic circuit have the advantages in the speed and current spike ? (20%)

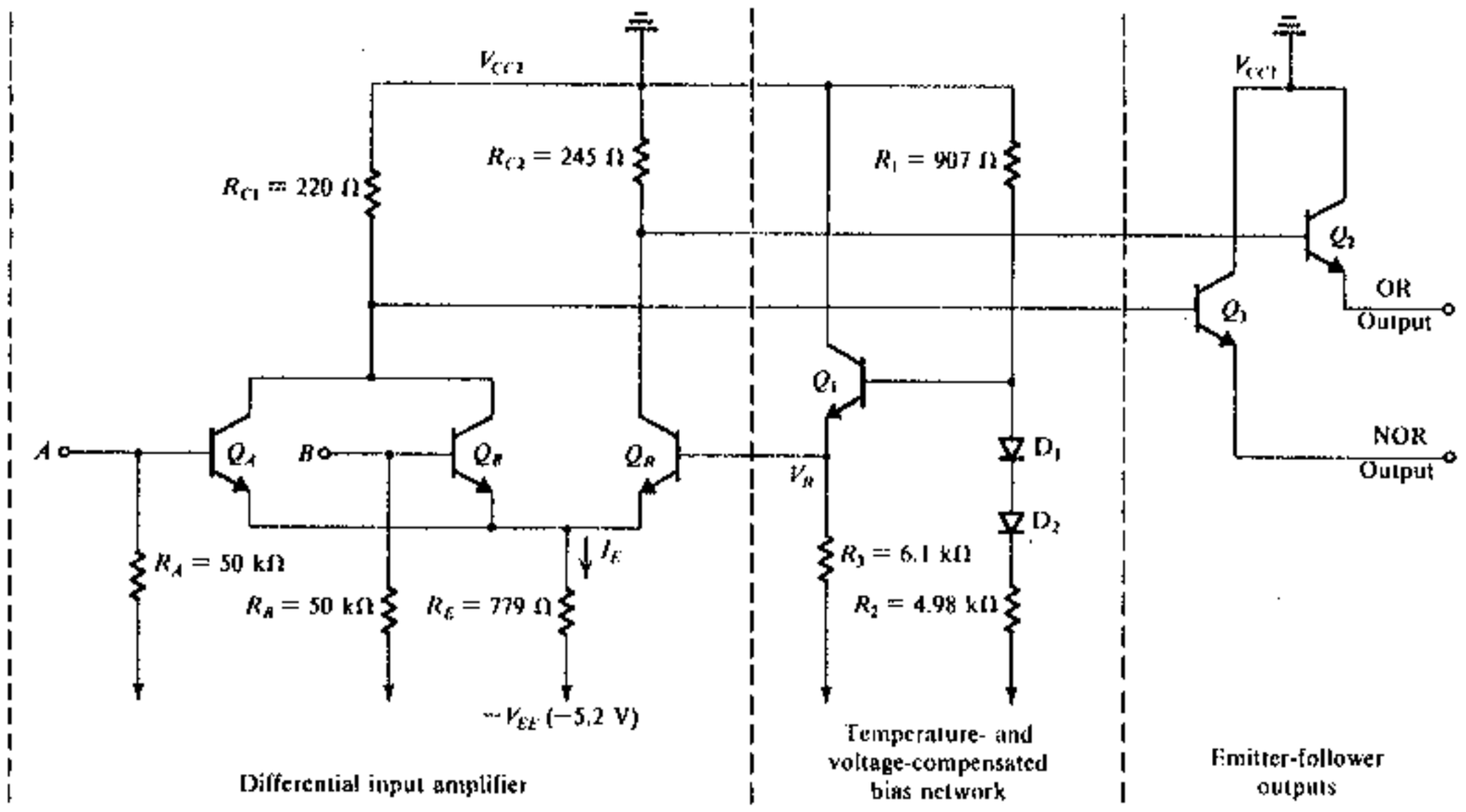

Fig. 5