國 立 清 華 大 學 命 題 紙

九十三學年度 動 機 系（所） 乙 組碩士班入學考試

科目 電路學及電子學 科號 1602 共 4 頁第 1 頁 *請在試卷【答案卷】內作答

1. A fully loaded $5-hp$ induction motor operates at 70 percent efficiency and a lagging power factor of 0.8. (One horsepower is approximately $745.7\ W$).
   (a) Find the average power and the reactive power delivered to the motor. (4%)
   (b) By what amount should the reactive power be decreased in order to achieve a power factor of at least 0.95. (4%)
   (c) It is decided to raise the power factor to 0.95 lagging by placing capacitance in parallel with the power line. Find the value of C required if the line voltage equals $480V$ rms and $f=60Hz$. (6%)

2. Fig 1 shows a Wheatstone bridge
   (a) Prove that the output voltage E_0 is proportional to the resistance change δR if $\frac{\delta R}{R} \ll 1$. Also find the proportional constant. (5%)
   (b) Design a circuit which can measure an inductance change. (Hint: Use an AC source as the bridge input and replace the resistors by appropriate electrical elements) (7%)

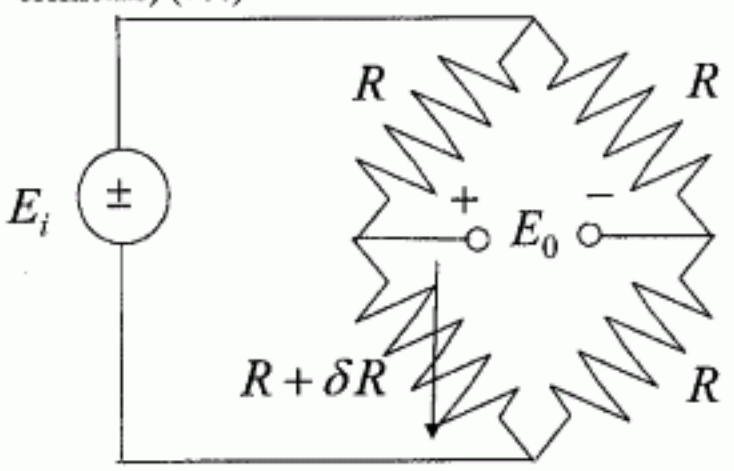

Fig. 1

3. If the switch in Fig. 2 has been closed for a long time before $t=0$ but is open at $t=0$, determine
   (a) the characteristic equation of the circuit, (4%)
   (b) i_x and v_R for $t>0$. (8%)

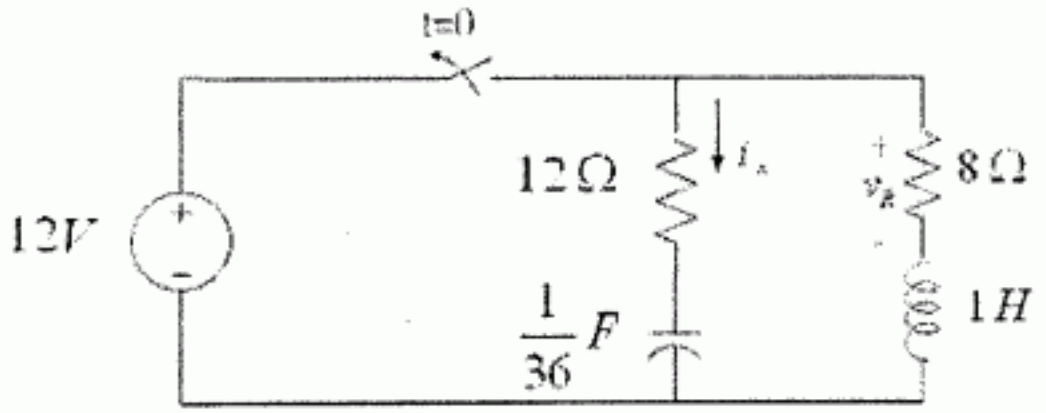

Fig. 2

4. For the circuit in Fig. 3, find the frequency response between V_i and V_0. Also draw the corresponding magnitude and phase plots. (12%)

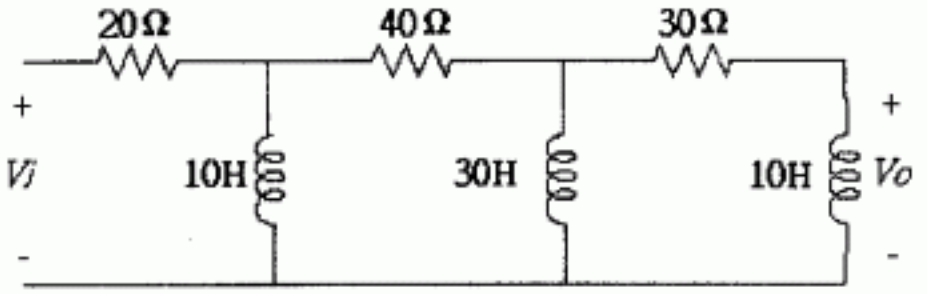

Fig. 3

5. Design a diode clamper to generate the output v_0 from the input v_1 shown in the figure if (a) V_γ=0, and (b) V_γ=0.7V. (10%)

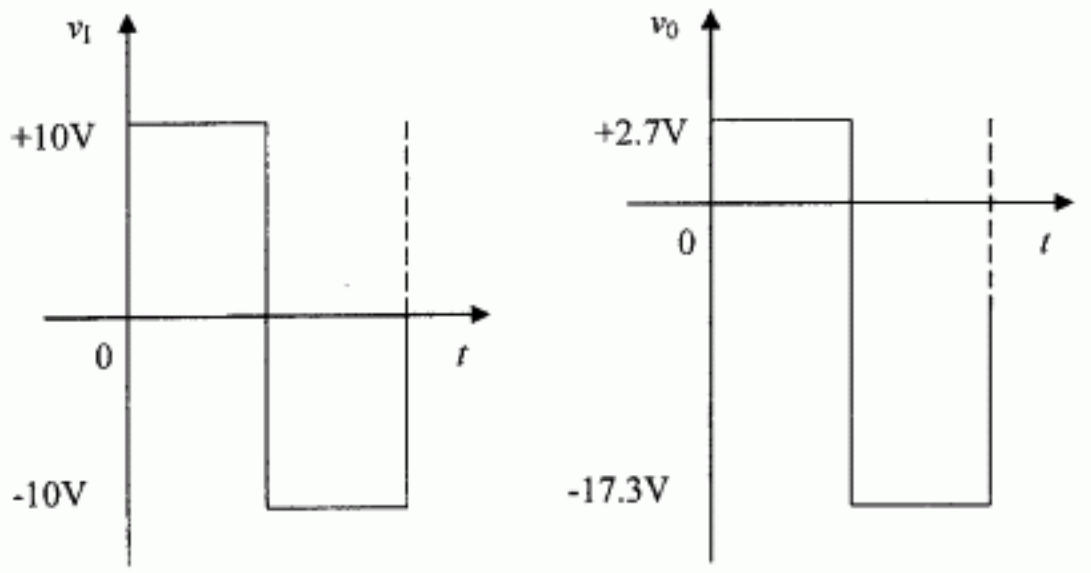

Fig. 4

6. Design a pnp common-emitter circuit such that I_{BQ}=15μA and V_{ECQ}=2.5V given the following parameters V_{BB}=2.5V, V_{CC}=5V, and βF=80. (10%)

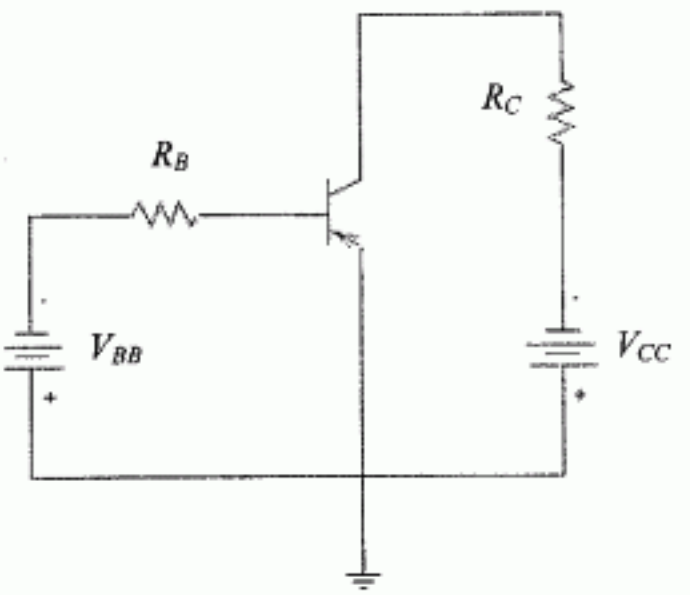

Fig. 5

7. For the circuit in the figure, the transistor parameters are: K_n=0.5mA/V^2, V_{TN}=2V, and λ=0. Determine the maximum value of C_L such that the bandwidth is at least BW=5MHz. State any approximations or assumptions that you make. (15%)

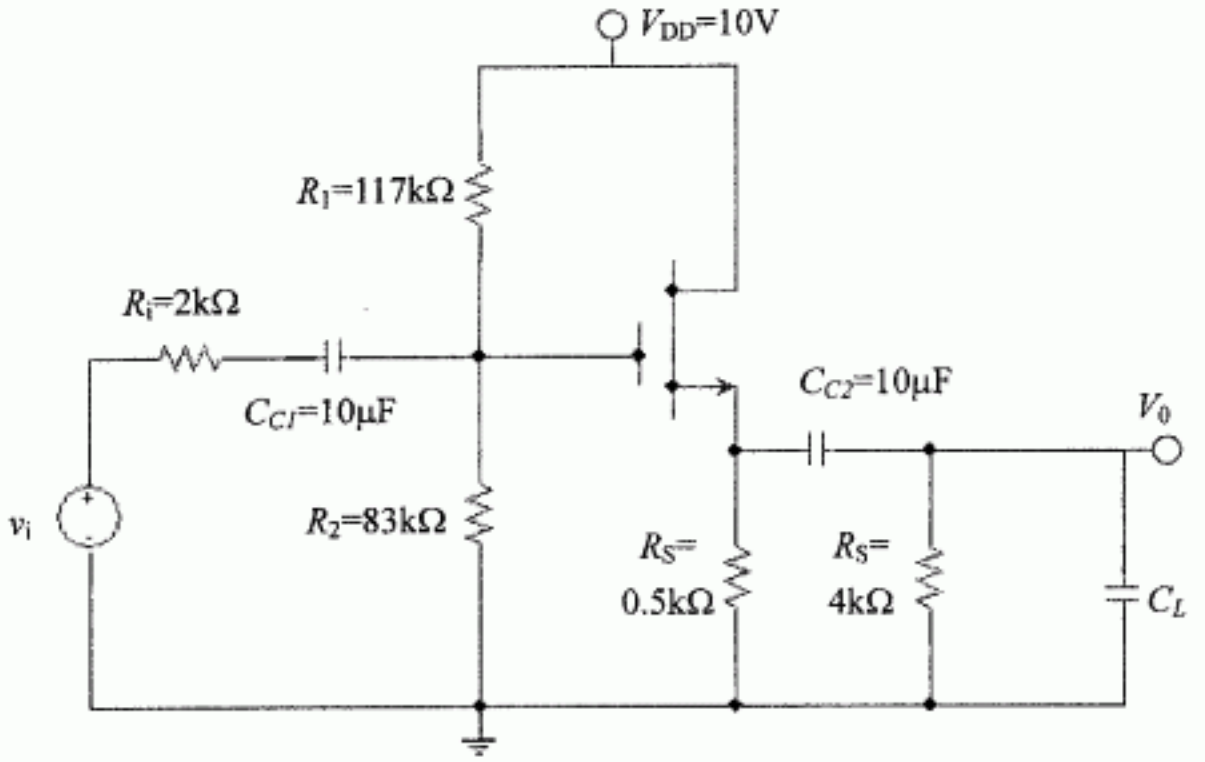

Fig. 6

8. For the amplifier in the figure, determine
   (a) the ideal closed-loop voltage gain (5%)
   (b) the actual closed-loop voltage if the open-loop gain is A_{od}=150,000 (5%)
   (c) the open-loop gain such that the actual closed-loop gain is within 1% of the ideal (5%)

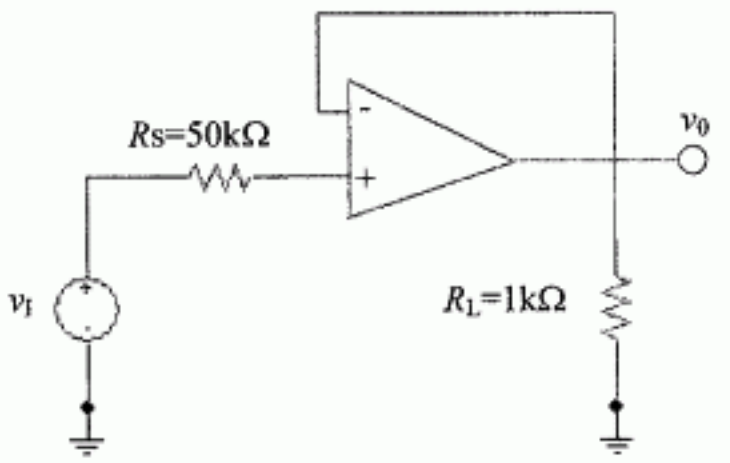

Fig. 7