國 立 清 華 大 學 命 題 紙

八十八學年度 動力機械工程學 系（所） 乙 組碩士班研究生招生考試

科目 電工學 科號 1302 共 3 頁第 一 頁 *請在試卷【答案卷】內作答

Note: Assume reasonable values for whatever data (e.g. α, β, h_{FE}) if necessary.

Prob.1 Explain why AC sources are economically more favorable over DC sources in domestic and industrial electric power supply. Are there any other advantages associated with using AC power? (12%)

Prob.2 Given a $12V$ voltage source, you are asked to design a divider circuit that drives an electrical appliance (, e.g., a CD player). It is known that the input voltage for this appliance has to be within $9 \pm 0.1V$ and its input impedance is $1 \pm 0.1M\Omega$. A possible configuration for this divider circuit is shown in Fig. 1. Do you think this circuit can accomplish the need? If the answer is yes, please explain why. If the answer is no, please suggest an alternative circuit that can satisfy the voltage requirement. (Notice that the maximum current acceptable for the $12V$ voltage source is $10mA$). (13%)

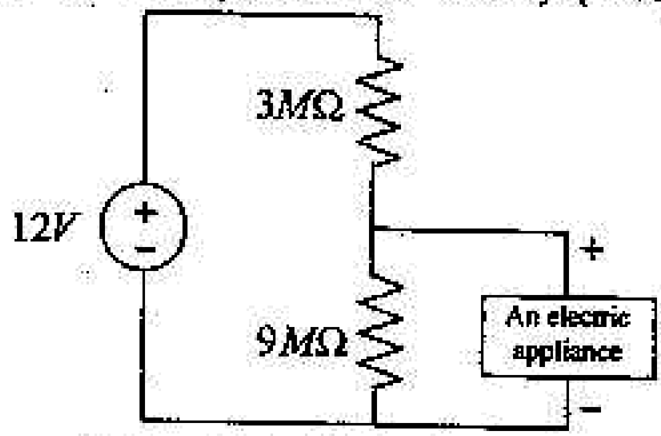

Fig.1: A voltage divider circuit for driving an electric appliance.

Prob.3 Linear differential transformers or so-called LVDT's are commonly used in motion control to provide measurements of displacement. As indicated in Fig. 2, the device basically consists of three coils and an iron core. The primary coil is energized from an external ac power source $e_{ex}(t)$, and the two secondary coils, connected together in phase opposition, are used as pickup coils. Due to the inductive coupling resulted from the presence of the iron core, an output voltage, $e_o(t)$ is generated across the two secondary coils. In this problem, you are asked to analyze the response characteristics of an LVDT.

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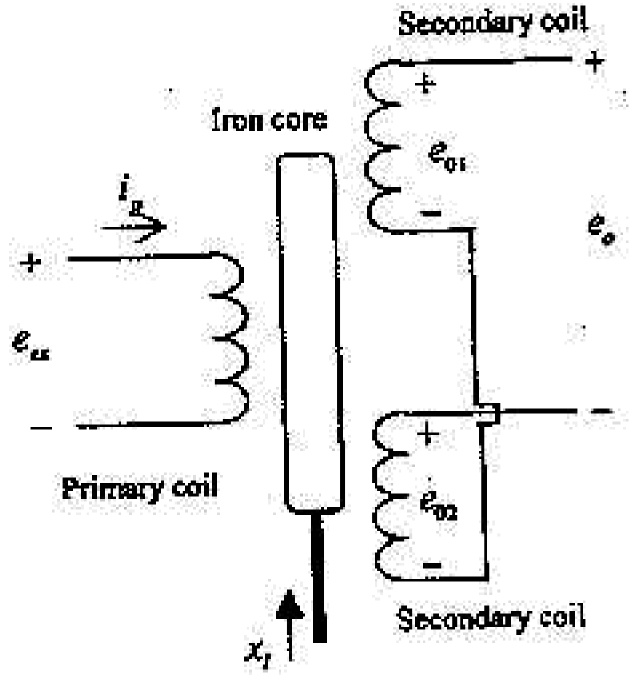

Fig. 2: Schematics of an LVDT

(i) The effect of mutual inductance plays an important role in the functioning of LVDT's. Please explain what mutual inductance effect is. (4%)

(ii) Assume that the current flowing in the primary coil is $i_p(t)$, the mutual inductance between the primary coil and the upper secondary coil equals M_1, and the mutual inductance between the primary coil and the lower secondary coil equals M_2. Please obtain the expressions for $e_{o1}(t)$ (the induced voltage across the upper secondary coil), $e_{o2}(t)$ (the induced voltage across the lower secondary coil), and $e_o(t)$. (5%)

(iii) Let the resistence of the primary coil be R_p. Referring to Fig. 2, find the frequency response from $E_i(j\omega)=\Im\{e_i(t)\}$ to $E_o(j\omega)=\Im\{e_o(t)\}$. Does the system have a phase lead or phase lag? (Notice that $\Im\{\}$ represents the Fourier transform of the time signal in the bracket.) (5%)

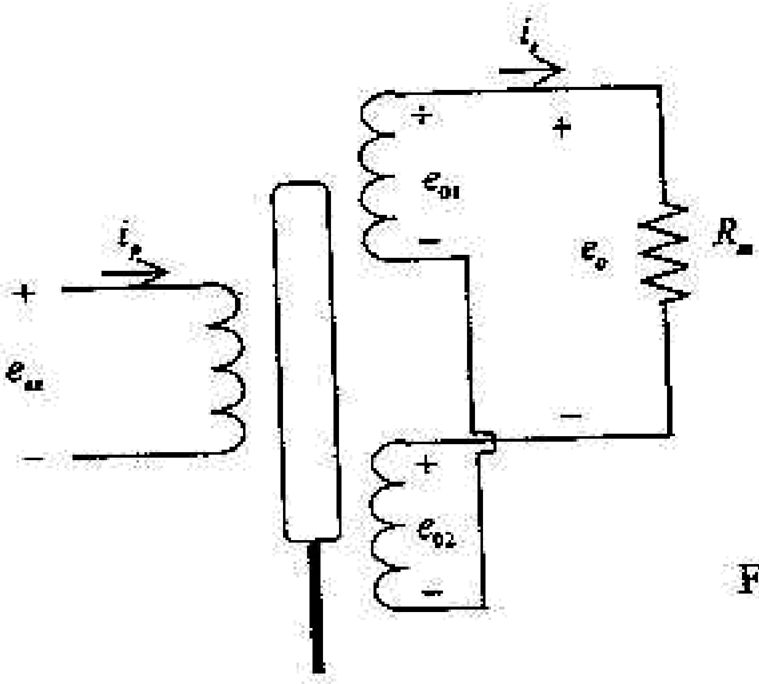

Fig.3: LVDT with an output resistor

(iv) If a resistor of R_m is attached to the output terminals as shown in Fig. 3, a current $i_s(t)$ will flow in the secondary coils. Obtain the two Kirchhoff's voltage laws for the primary coil and the secondary coils respectively. You may want to assume that the primary coil, in addition to the coil resistance R_p, also has an self-inductance of L_p, and each secondary coil has a self-inductance L_s and a coil resistance R_s. Do not forget to consider the mutual inductance effect. (6%)

(v) Find the frequency response from $E_i(j\omega)=\Im\{e_i(t)\}$ to $E_o(j\omega)=\Im\{e_o(t)\}$ for the scenario described in part (iv). (5%)

Prob.4 (a) Perform a DC analysis of the following Biploar-Junction-Transistor Darligton circuit as shown in Fig. 4, calculate I_{E1}, I_{E2}, I_{B1}, r_{e1}, r_{e2}, with V_{BE} =0.7 V, β_{dc}= 100 and β = 100 for both transistors. (5%)

(b) Continuing from (a), if a small signal is fed into the input terminal A, then calculate and plot the output waveform at terminal B. (5%)

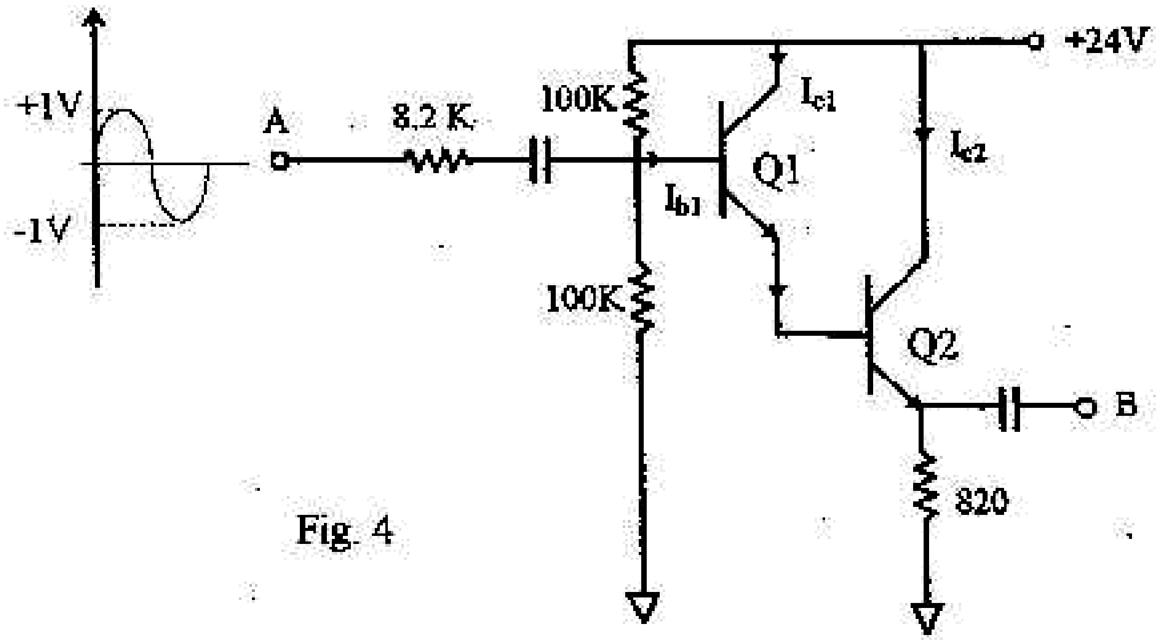

Fig. 4

Prob.5 Consider a single OPAMP circuit as shown in Fig. 5.

(a) If we assume that the OPAMP is an ideal one, with the input at terminal A, calculate and plot the output waveform at terminal B. (5%)

(b) Now, if a more realistic analysis of this circuit is requested, with A_v = 100,000 V/V, r_{in} = 2 MΩ , r_{out}= 75Ω , find the closed loop input impedance and output impedance. (4%)

(c) Continuing from (b), if $I_{in(bias)}$ =80 nA, $I_{in(offset)}$ =20 nA, $V_{in(offset)}$ =2mV, calculate the output offset voltage (4%)

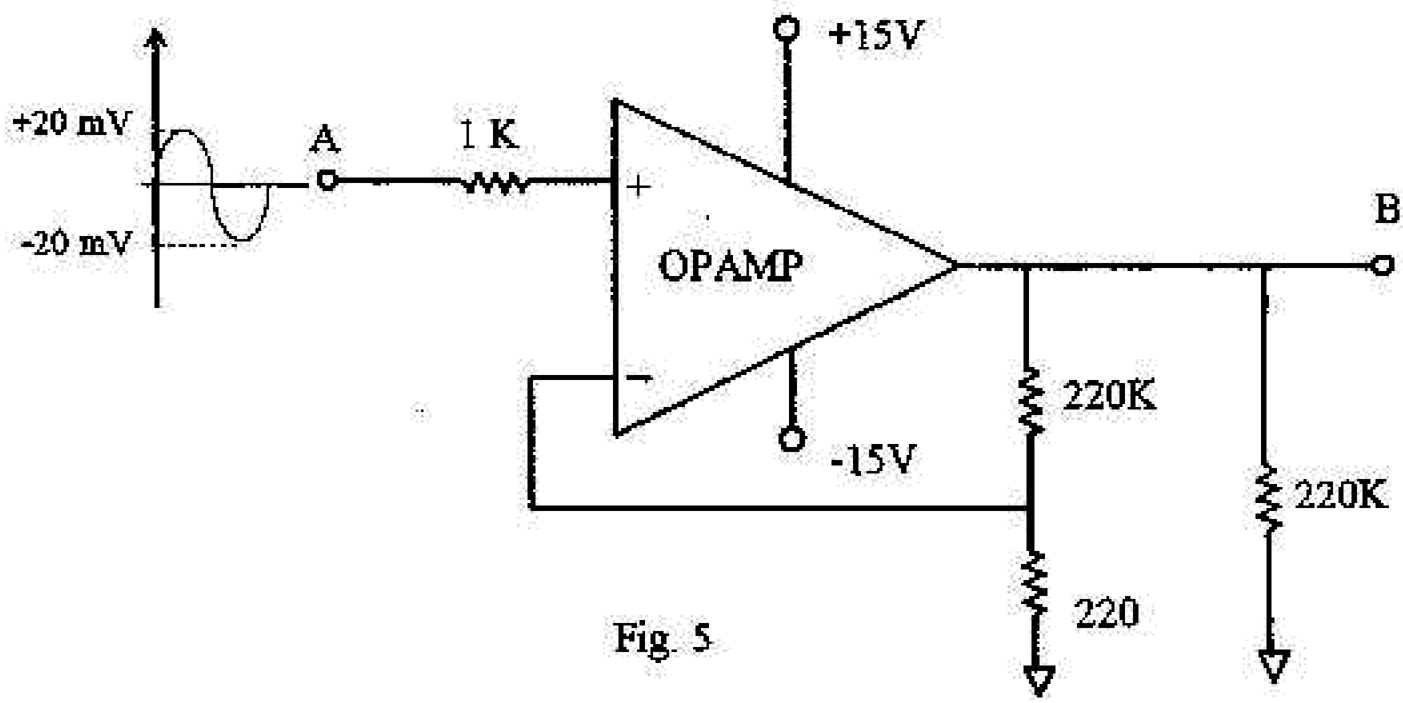

Fig. 5

Prob.6 (a) CompareTTL(Transistor-Transistor-Logic),CMOS(Complementary-Metal-Oxide-Semi-conductor) and ECL(Emitter-Coupled-Logic) devices from gate delay, bandwidth, power consumption, noise margin, component cost, fan out and driving capability. (7%)

(b) Draw the truth table of RS Flip-Flop, JK Flip-Flop, D Flip-Flop and T Flip-Flop. Describe their functionality by a specific example, respectively. (8%).

Prob.7 Consider the decoder circuit with three negative edge trigger JK Flip-Flops as shown in Fig.6. If a series of clock pulses is applied to the terminal A, complete the timing diagram of Q1, Q2 and Q3, respectively.(12%)

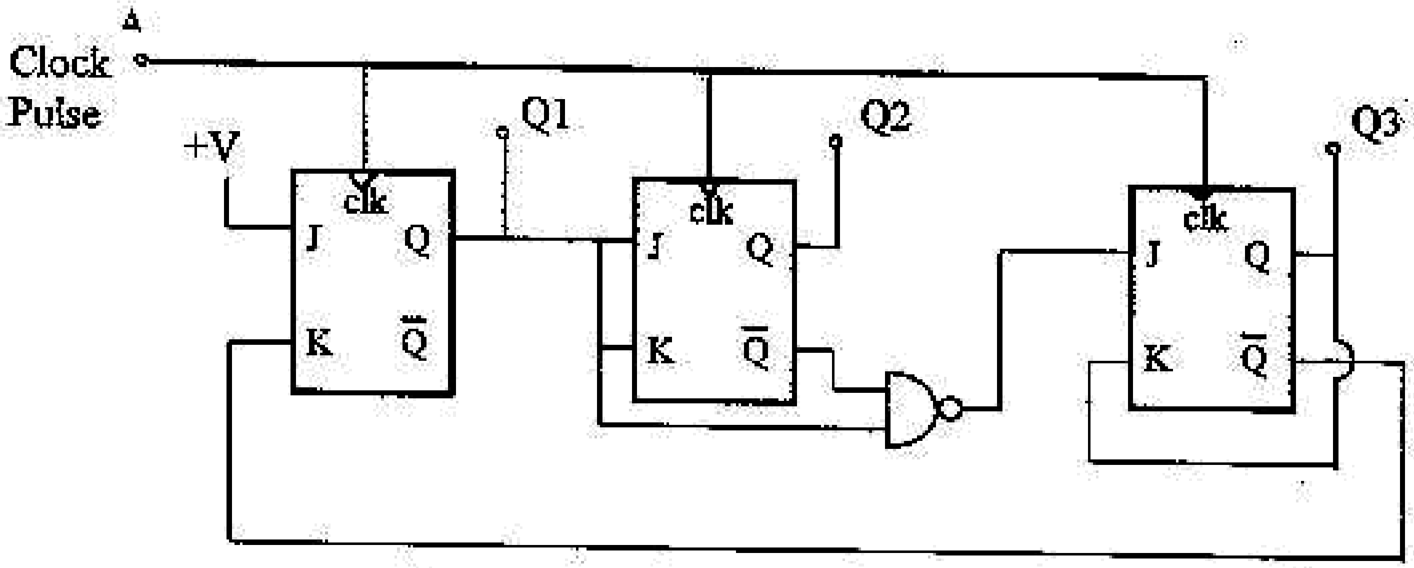

Fig. 6