國立清華大學 100 學年度碩士班入學考試試題

系所班組別：動力機械工程學系乙組(電控組)

考試科目（代碼）：電路學及電子學 (1102)

Notice: To have full credits, you should describe your approximation and assumptions, write down every essential equation, and give properly explanation in solving problems.

1. Choose the one alterative that best completes the statement or answers the question. One point for each correct answer. (10 pts)

(a) A network has 10 branches and 8 nodes, then how many independent loops would it be?
A) 2　B) 3　C) 17　D) 18　E) not enough information.

(b) The Wheatstone bridge circuit is widely used to measure:
A) exact voltages.　B) precise resistances.　C) accurate currents.
D) precise power.　E) all the these.

(c) A resistor with negative resistance, implies that
A) It will still dissipate power.　B) It can deliver power.
C) It has a positive voltage drop. D) It will reduce current flow. E) none of these.

(d) If a circuit element is measured to have i=sin10t and v=cos10t, the element is
A) a resistor.　B) a capacitor.
C) an inductor.　D) none of these.　E) all of these.

(e) Electrolytic capacitor differ from all other capacitors in construction in that they are:
A) larger.　B) smaller.
C) sensitized.　D) polarized.　E) none of these.

(f) If a 22 μF and 100 μF capacitor are connected in series with a 15V source, the total capacitance equals_____and the 22 μF capacitor drops_____.
A) 122μF, 15V.　B) 18μF, 12.30V.
C)18μF, 2.7V.　D) 18μF, 15V.　E) none of these.

(g) In a series RLC circuit while operating below the resonant frequency, the impedance is:
A) mode capacitive.　B) more inductive.
C) at minimum.　D) at maximum.　E) none of these.

(h) What is the source voltage in a series resonant circuit if $\mathbf{V_c}$ = 150V, $\mathbf{V_L}$ = 100V and $\mathbf{V_R}$ = 50V?
A) 300V.　B) 100V.　C) 70.71V.
D) 35.35V.　E) none of these.

(i) What is the bandwidth of a series resonant circuit if the resonant frequency is 14.2 MHz, the inductive reactance is 2 kΩ and the coil's resistance is 8Ω?

A) 8.8 kHz.　　B) 1.42 kHz.
C) 2.84 kHz.　　D) 5.68 kHz.　　E) none of these.

(j) If the true power is 100W and the reactive power is 100 VAR (Ind.), the power factor is:

A) 0.707 leading.　　B) 0.707 lagging.
C) 0.5 leading.　　D) 0.5 lagging.　　E) none of these.

2. Fill the blanks for the following questions: (10 pts. 1 pt for each blank)

(a) The characteristics of ideal operational amplifier are (A), zero common-mode gain, (B), and infinite bandwidth.

(b) Moore's law describes that transistor density of semiconductor chips would be (C) roughly every (D) months.

(c) Diodes can be combined with resistors to form a (E) circuit that converts an ac voltage into one that is limited to one polarity.

(d) A (F) forms between two regions if a piece of intrinsic silicon is doped so that half is n-type and the other half is p-type.

(e) (G) means that a voltage produced from the action of photons in a solar cell.

(f) The characteristics for Source Follower are high input resistance, (H), (I), and relatively large current gain.

(g) Field-effect transistors, FETs, are solid-state devices in which an (J) controls the flow of charge carriers through a conducting channel.

3. For the following bridge circuit as shown in Figure 3. (10 pts)

(a) Determine R_x to make $I=0$.

(b) If R_x is 4 kΩ, calculate I.

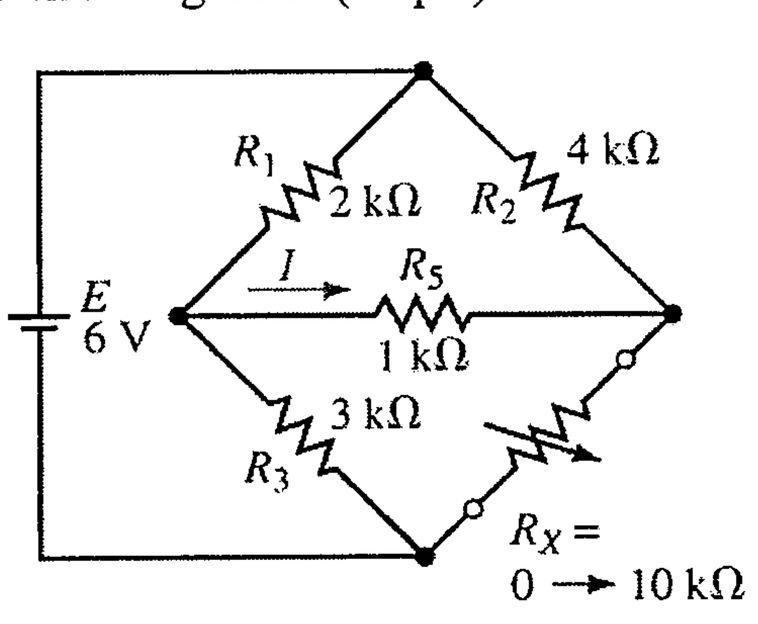


Figure 3

4. As shown in Figure 4, the neon light fires when its voltage reaches 60V and turn off when its voltage drops to 30V. Its resistance is 120Ω when on and infinitively large when off. (10 pts)

(a) For how long is the lamp on each time the capacitor discharges?

(b) What is the time interval between light flashes?

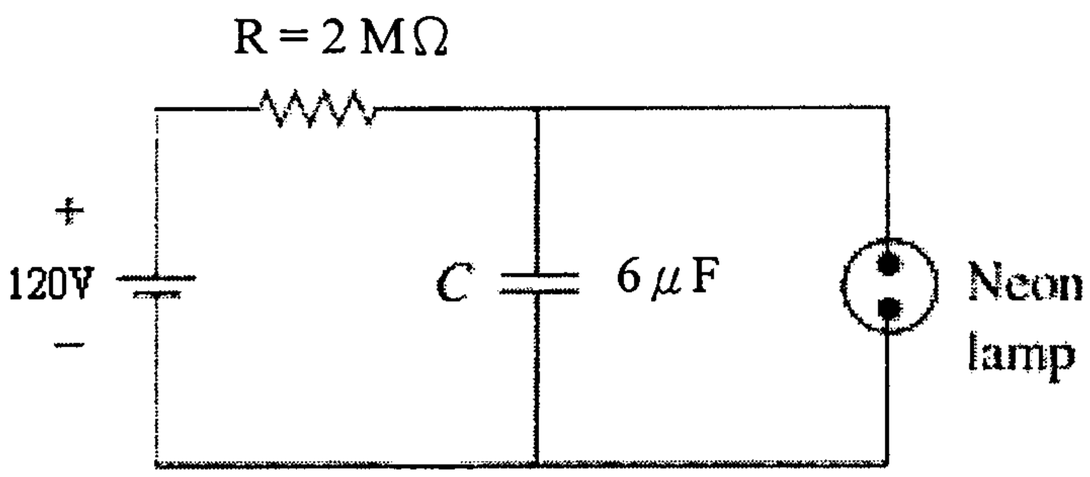


Figure 4

5. A 120-V rms 60-Hz source supplies two loads connected in parallel, as shown in Figure 5. (15 pts)

(a) Find the power factor of the parallel combination.

(b) Calculate the value of the capacitance connected in parallel that will raise the power factor to unity.

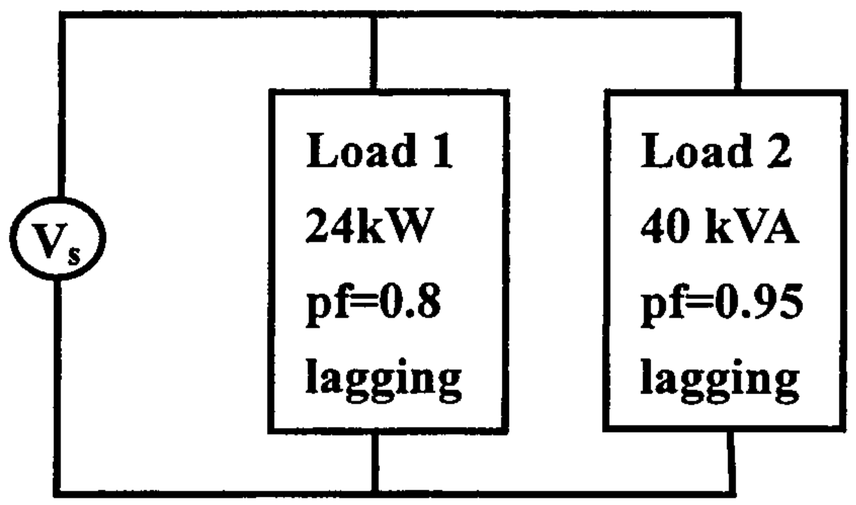


Figure 5

6. Derive the differential equation for the output v_O of op-amp circuit shown in Figure 6. (10 pts)

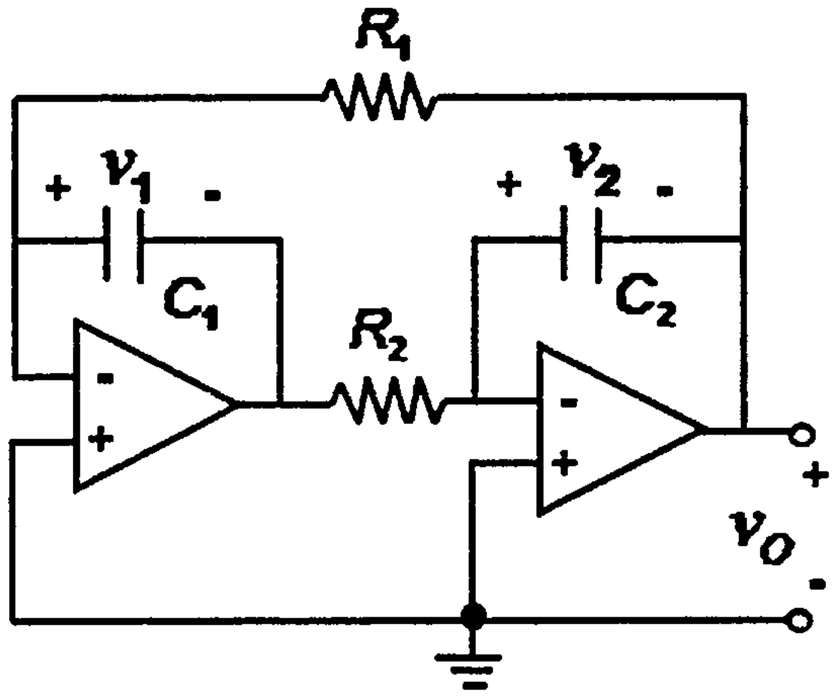


Figure 6

7. The parameters of the transistor in the circuit in Figure 7 are $\beta = 100$ and Early voltage $V_A = \infty$.
   (a) Determine R_1 and R_2 to obtain a bias-stable circuit; that is $R_1 \| R_2 = 0.1(1+\beta)R_E$, with the Q-point in the center of the load line, $R_C = 0.8\ \text{k}\Omega$ and $R_E = 0.2\ \text{k}\Omega$. (9 pts)
   (b) Derive the small-signal voltage gain $A_v = v_O/v_S$. (Please DO NOT calculate the voltage gain; only derive the expression.) (6 pts)

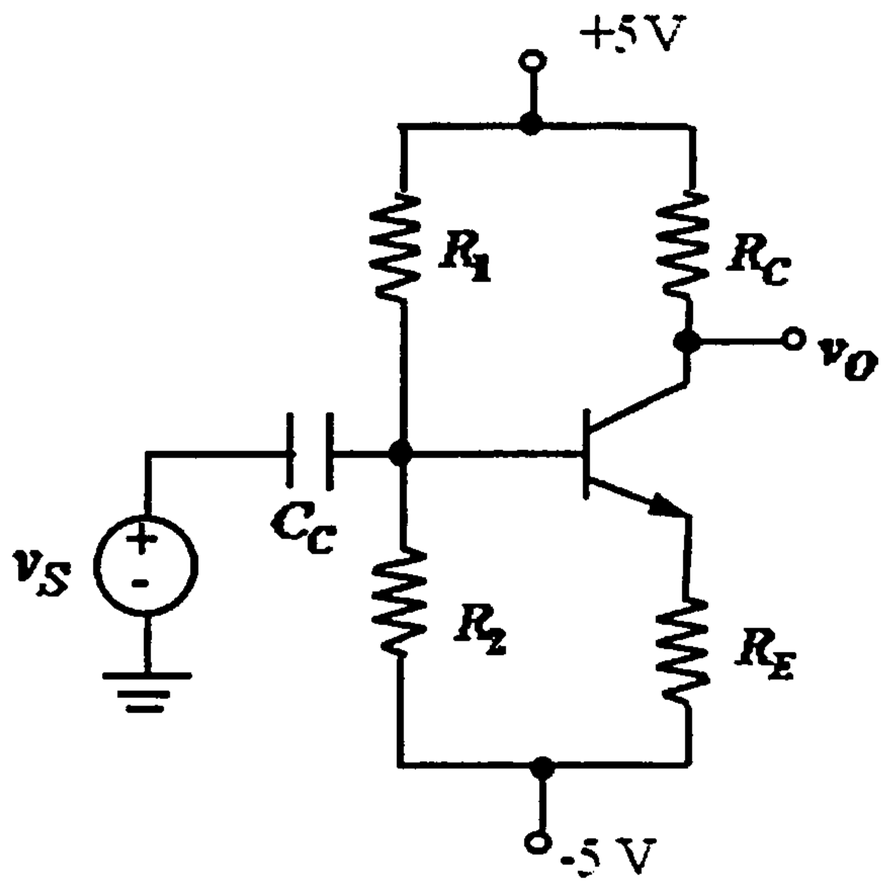
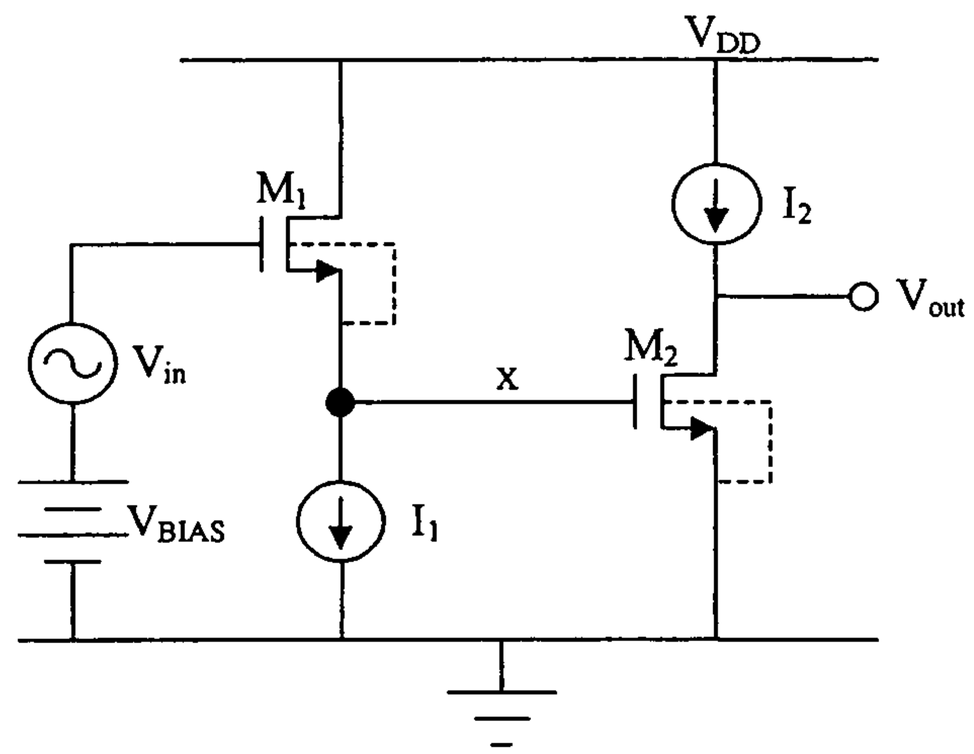


Figure 7

8. For the circuit shown in Figure 8, assume $g_{m1} >> 1/r_{o1}$. The source and bulk of M_1 are connected. M_1, M_2 are in saturation.
   (a) Write an expression for the small signal gain of entire circuit, v_{out}/v_{in}. (4 pts)
   (b) Given that V_{th} = 1 V, $g_{m1} = g_{m2}$ = 1 ms, $I_1 = I_2$ = 150 μA. What is the value of V_{BIAS}? (Hint: One of the three expressions for transconductance is very useful for this problem.) (6 pts)

Figure 8



9. As shown in Figure 9, all devices are operating in saturation. Ignore all capacitances except C_L. Body of $M1$, $M2$ at ground. $M1 = M2$, $M3 = M4 = M5$.
   (a) Draw the small-signal equivalent model. (4 pts)
   (b) Derive an expression for output voltage gain, v_{out}/v_{in}. (6 pts)

Figure 9